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Exp	Experiment 16 :Comon Drain Differential amplifier				
Experiment 17 :R-2R DAC					
	·				

Note : Remove "Table of Content" before including in CP Book

15ECL77 : VLSI LAB

A. LABORATORY INFORMATION

1. Lab Overview

Degree:	B.E	Program:	EC
Year / Semester :	4 / 7	Academic Year:	2018-19
Course Title:	VLSI Lab	Course Code:	15ECL77
Credit / L-T-P:	2 / 0-1-2	SEE Duration:	180 Minutes
Total Contact Hours:	40 Hrs	SEE Marks:	80 Marks
CIA Marks:	20	Assignment	1 / Module
Course Plan Author:	Mrs. Shilpa Rani P	Sign	Dt :
Checked By:	Mr.	Sign	Dt :

2. Lab Content

Unit	Title of the Experiments		Concep	Blooms
		Hours	t	Level
1	Write Verilog Code for the following circuits and their Test	3	Basic	L4
	Bench for verification, observe the waveform and synthesize		VLSI	Analyze
	the code		circuits	
	i. An inverter		synthesi	
	ii. A Buffer		s	
	iii. Transmission Gate			
2	Write Verilog Code for the following circuits and their Test	3	Logic	L4
	Bench for verification, observe the waveform and synthesize		Gates	
	the code		synthesi	
	iv. Basic/universal gates		s	
3	Write Verilog Code for the following circuits and their Test	3	Flip-flop	L4
	Bench for verification, observe the waveform and synthesize		synthesi	
	the code		s	
	v. Flip flop –RS, D, JK, MS, T			

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4	Write	Verilog Cod	e for the following circuits and their Test	3	Adders	L4	
	Bench	for verifica	tion, observe the waveform and synthesize		and		
	the co	ode			counters		
	vi. Se	rial & Parallel	adder		synthesi		
	VII. 4-	-bit counter [Synchronous and Asynchronous counter]	2	S		
5	Write Verilog Code for the following circuits and their lest			3	SAR	L4	
	Bencr	n for verifica ada	tion, observe the waveform and synthesize		synthesi		
	the co	ode			S		
<u> </u>	VIII. S	uccessive app	proximation register [SAR]	<u> </u>	CMOC		
6	Desig	n an Inverter	with given specifications**, completing the	6	CMOS	L4	
	aesig	n flow			Inverter		
	ment	ioned below:	a the second second for the second second		design		
	a. Dra	aw the schem	atic and verify the following				
		Analysis					
		instent Analy	sis				
	D. Dra	aw the Layou	t and verify the DRC, ERC				
	d Ev	etract PC an	d back annotate the same and verify the				
	Desig	in act inc and	u back annotate the same and verify the				
		rify & Ontim	ize for Time Power and Area to the given				
	const	raint*	ize for thine, rower and filed to the given				
7	Desig	n the (i) Cor	mmon source and Common Drain amplifier	9	CMOS	L4	
-	and (i	ii) A Sinale		2	Aplifiers		
	Stage	differential	amplifier, with given specifications**.		Desian		
	comp	leting the			J		
	desig	n flow mentio	oned below:				
	a. Dra	aw the schem	atic and verify the following				
	i) DC	Analysis					
	ii) AC	Analysis					
	iii) Tr	ansient Analy	vsis				
	b. Dra	aw the Layou	t and verify the DRC, ERC				
	c. Ch	eck for LVS					
	d. Ex	tract RC and	d back annotate the same and verify the				
	Desig	n.					
8	Desig	n an op-an	np with given specification** using given	3	CMOS	L4	
	differ	ential amplifi	er		OPAMP		
	Comr	non source	and Common Drain amplifier in library***		Design		
	and completing the design flow mentioned below:						
	a. Dra	aw the schem	atic and verify the following				
	i) DC	Analysis					
	ii). AC	C Analysis					
	iii) Tr	ansient Analy	vsis				

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Title: Course Lab Manual Page: 4 / 37 Copyright ©2017. cAAS. All rights reserved. b. Draw the Layout and verify the DRC, ERC
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b. Draw the Layout and verify the DRC, ERC
c. Check for LVS
d. Extract RC and back annotate the same and verify the
Design.
9 Design a 4 bit R-2R based DAC for the given specification and 3 R-2R L4
completing the based
design flow mentioned using given op-amp in the library***. DAC
a. Draw the schematic and verify the following Design
i) DC Analysis
ii) AC Analysis
iii) Transient Analysis
b. Draw the Layout and verify the DRC, ERC
10For the SAR based ADC mentioned in the figure below draw3SARL4
the mixed signal based
schematic and verify the functionality by completing ASIC ADC
Design FLOW. Design
[Specifications to GDS-II]
Comparator high when
Viest
Output
bh
Approximation Register
teset

3. Lab Material

Unit	Details	Available
1	Text books	
	Dept Lab Manual	In Dept Library
2	Reference books	
	1. Digital Logic Applications and Design, John M Yarbrough, Thomson	In College Library
	Learning, 2001. ISBN 981-240-062-1.	
	2. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and	In College Library
	Synthesis",	
	Pearson Education, Second Edition.	

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3. "Basic VLSI Design" - Douglas A. Pucknell& Kamran Eshraghian, PH		In College Library		
3 rd Edition (original Edition – 1994)		l Edition – 1994)		
3	Other	s (Web, Video	o, Simulation, Notes etc.)	

4. Lab Prerequisites:

-	_	Base Course:		_	-
SNo	Course	Course Name	Topic / Description		Remarks
	Code				
1	15EC33	Digital Elecronics	Logic Gates, Flip-flops, Adders	3	
2	15EC53	Verilog HDL	Gate-Level Modeling,Dataflow	5	
			Modeling, Behavioral Modeling		
3	15EC63	VLSI Design	CMOS circuit Design, Stick diagrams	6	
			and Layout		

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

5. General Instructions

SNo	Instructions	Remarks
1	Observation book and Lab record are compulsory.	
2	Students should report to the concerned lab as per the time table.	
3	After completion of the program, certification of the concerned staff in-	
	charge in the observation book is necessary.	
4	Student should bring a notebook of 100 pages and should enter the	
	readings /observations into the notebook while performing the	
	experiment.	
5	The record of observations along with the detailed experimental	
	procedure of the experiment in the Immediate last session should be	
	submitted and certified staff member in-charge.	
6	Should attempt all experiments given in the list session wise.	
7	It is responsibility to create a separate directory to store all the	
	programs, so that nobody else can read or copy.	
8	When the experiment is completed, should shut down the system	
	properly.	
9	Any damage of the equipment or burn-out components will be viewed	
	seriously either by putting penalty or by dismissing the total group of	
	students from the lab for the semester/year	
10	Completed lab assignments should be submitted in the form of a Lab	
	Record in which you have to write the algorithm, program code along	

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with comments and output for various inputs given

6. Lab Specific Instructions

SNo	Specific Instructions	Remarks
1	Start computer	
2	Open the text editor	
3	Select new file.	
4	Write the program	
5	Save the program with .v extension.	
6	Compile the program	
7	Execute the program	

B. OBE PARAMETERS

1. Lab / Course Outcomes

#	COs	Teach.	Concept	Instr	Assessment	Blooms'
		Hours		Method	Method	Level
1	Simulate and synthesize basic VLSI	3	Basic VLSI	Demons	Slip Test	L4
	circuits		circuits	tration/		
	using Verilog coding		synthesis	Practica		
				I		
2	Simulate and synthesize logic Gates	3	Logic Gates	Practica	Slip Test	L4
	using Verilog coding		synthesis	I		
3	Simulate and synthesize flip-flops	3	Flip-flop	Practica	Slip Test	L4
	using Verilog coding		synthesis	I		
4	Simulate and synthesize adders and	3	Adders and	Practica	Slip Test	L4
	counters using Verilog coding		counters	I		
			synthesis			
5	Simulate and synthesize SAR using	3	SAR	Practica	Slip Test	L4
	Verilog coding		synthesis	I		
6	Design CMOS Inverter schematic ,	6	CMOS	Demons	Slip Test	L4
	Layout and verify LVS.		Inverter	tration/		
			design	Practica		
				I		
7	Design CMOS Amplifier schematic ,	9	CMOS	Practica	Slip Test	L4
	Layout and verify LVS.		Aplifiers	I		
			Design			
8	Design Op-amp using differential	3	CMOS	Practica	Slip Test	L4
	amplifier and CDA schematic , Layout		OPAMP	I		
	and verify LVS.		Design			
9	Design R–2R DAC schematic, Layout	3	R-2R based	Practica	Slip Test	L4

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	and verify DRC, ERC		DAC Design	I		
10	Draw mixed signal schematic and verify	3	SAR based	Practica	Slip Test	L4
	its functionality of SAR based ADC		ADC Design	I		
-	Total	39	-	-	-	-

Note: Identify a max of 2 Concepts per unit. Write 1 CO per concept.

2. Lab Applications

SNo	Application Area	CO	Level
1	Static RAM, Image sensors	CO1	L4
2	Alarm switch, Temperature detector, Door bell switch	CO2	L4
3	Data storage, data trasfer, registers, counters, frequency division	CO3	L4
4	Designing ALU, Fast multipilers, Digital clocks, Multiplexing, Parallel to serial	CO4	L4
	data conversion		
5	Analog to digital conversion, PLC application	CO5	L4
6	Data converters, Transceivers	CO6	L4
7	FET, Oscilloscopes, Electronic voltmeters, operational aplifiers	C07	L4
8	Voltage summer, Integrators, digital to analog connversion	CO8	L4
9	Motor control, digital potentiometers, Software Radio, Data distribution	CO9	L4
	system		
10	Temperature sensors, bus architecture in microcontroller, distance locator	CO10	L4

Note: Write 1 or 2 applications per CO.

3. Articulation Matrix

(CO – PO MAPPING)

_	Course Outcomes	Program Outcomes												
#	COs	PO	PO	PO	PO	PO	PO	PO	PO	PO	PO	PO	PO	Level
		1	2	3	4	5	6	7	8	9	10	11	12	
15ECL77.1	Simulate and synthesize basic	3	1			3				3				L4
	VLSI circuits													
	using Verilog coding													
15ECL77.2	Simulate and synthesize logic	3	1			3				3				L4
	Gates													
	using Verilog coding													
15ECL77.3	Simulate and synthesize flip-	3	1			3				3				L4
	flops													
	using Verilog coding													
15ECL77.4	Simulate and synthesize adders	3	1			3				3				L4
	and counters using Verilog													
	coding													
15ECL77.5	Simulate and synthesize SAR	3	1			3				3				L4

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	using Verilog coding								
15ECL77.6	Design CMOS Inverter schematic	3	2	1	3		3		L4
	, Layout and verify LVS.								
15ECL77.7	Design CMOS Amplifier	3	2	1	3		3		L4
	schematic , Layout and verify								
	LVS.								
15ECL77.8	Design Op-amp using	3	2	1	3		3		L4
	differential amplifier and CDA								
	schematic , Layout and verify								
	LVS.								
15ECL77.9	Design R-2R DAC schematic,	3	2	1	3		3		L4
	Layout and verify DRC, ERC								
15ECL77.1	Draw mixed signal schematic	3	2	1	3		3		L4
0	and verify its functionality of								
	SAR based ADC								
	Average	3	1.5	0.5	3		3		

Note: Mention the mapping strength as 1, 2, or 3

4. Mapping Justification

Маррі	Mapping Mar		Justification
		Level	
СО	РО	-	-
C01	PO1	3	Knowledge of basic VLSI circuits is required for understanding complex VLSI problems
C01	PO2	1	Knowledge of basic VLSI circuits is required for problem analysis in VLSI designs.
CO1	PO5	3	Simulation of basic VLSI circuits requires tools like "xilinx"
C01	PO9	1	Individual and team work is required for simulation of basic VLSI circuits.
CO2	PO1	3	Knowledge of logic gates is required for understanding complex VLSI problems
CO2	PO2	1	Knowledge of logic gates is required for problem analysis in VLSI designs.
CO2	PO5	3	Simulation of logic gate circuits requires tools like "xilinx"
CO2	PO9	1	Individual and team work is required for simulation of logic gates.
CO3	PO1	3	Knowledge of flip–flops is required for understanding complex VLSI problems
CO3	PO2	1	Knowledge of flip-flops is required for problem analysis in VLSI designs.
CO3	PO5	3	Simulation of flip-flop circuits requires tools like "xilinx"
CO3	PO9	1	Individual and team work is required for simulation of Flip-flops

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CO4	PO1	3	Knowledge of adders is required for under problems	standing complex VLSI
CO4	PO2	1	Knowledge of adders is required for problem a	nalysis in VLSI designs.
CO4	PO5	3	Simulation of adder circuits requires tools like	"xilinx"
CO4	PO9	1	Individual and team work is required for simul	ation of adders
CO5	PO1	3	Knowledge of SAR is required for understar convertion	nding analog to digital
CO5	PO2	1	Knowledge of SAR is required for problem ana	lysis in VLSI designs.
CO5	PO5	3	Simulation of SAR circuit requires tools like "xi	linx"
CO5	PO9	1	Individual and team work is required for simul	ation of SAR
CO6	PO1	3	Knowledge of CMOS Inverter is required for VLSI problems	understanding complex
CO6	PO2	2	Knowledge of CMOS Inverter is required for p designs.	problem analysis in VLSI
CO6	PO3	1	Designing of CMOS Inverter is required for d VLSI circuits	evelopment of complex
CO6	PO5	3	Design of CMOS Inverter requires "cadence" or	"tanner tools" usage.
CO6	PO9	2	Individual and team work is required for design	n of CMOS Inverter
C07	PO1	3	Knowledge of CMOS Amplifiers is required amplification related problems	ired for solution of
C07	PO2	2	Knowledge of CMOS Amplifiers is required f	or problem analysis in
C07	PO3	1	Designing of CMOS Amplifiers is required complex VLSI circuits	d for development of
C07	PO5	3	Design of CMOS Amplifiers requires "cadence"	or "tanner tools" usage.
C07	PO9	2	Individual and team work is required for desig	n of CMOS Amplifiers
CO8	PO1	3	Knowledge of Op-amp is required for solution problems	of amplification related
CO8	PO2	2	Knowledge of Op-amp is required for pro	blem analysis in VLSI

			designs.
CO8	PO3	1	Designing of Op-amp is required for development of complex VLSI
			circuits
CO8	PO5	3	Design of Op-amp requires "cadence" or "tanner tools" usage.
CO8	PO9	2	Individual and team work is required for design of Op-amp
CO9	PO1	3	Knowledge of DAC is required for solving signal conversion related
			problems
CO9	PO2	2	Knowledge of DAC is required for problem analysis in VLSI designs.
CO9	PO3	1	Designing of DAC is required for development of complex VLSI

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CO10	PO1	1	3	Knowledge of SAR is required for solving signal	conversion related
				problems	
CO10	PO2	Ź	2	Knowledge of SAR is required for problem analysis	in VLSI designs.
CO10	PO3	1	l	Designing of SAR is required for development of co	omplex VLSI circuits
CO10	PO5	3	3	Design of SAR requires "cadence" or "tanner tools"	usage.
CO10	PO9	Ź	2	Individual and team work is required for design of	SAR

Note: Write justification for each CO-PO mapping.

5. Curricular Gap and Content

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					

Note: Write Gap topics from A.4 and add others also.

6. Content Beyond Syllabus

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					

Note: Anything not covered above is included here.

C. COURSE ASSESSMENT

1. Course Coverage

Unit	Title	Teachi		No. of question in Exam						CO	Levels
		ng	CIA-	CIA-	CIA-	Asg-	Asg-	Asg-	SEE		
		Hours	1	2	3	1	2	3			
1	Inverter, Buffer, TG	03	1	-	-	1	-	-	1	CO1	L4
2	Logic gates	03	1	-	-	1	-	-	1	CO2	L4
3	Flip-flops	03	1	-	-	1	-	-	1	CO3	L4
4	Adders, Counters	03	1	-	-	1	-	-	1	CO4	L4
5	SAR	03	1	_	_	1	-	-	1	CO5	L4

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6	CMOS Inverter Schematic			03	-	1	-	-	1	-	1	CO6	L4
7	CMOS Inverter Layout			03	-	1	_	_	1	-	1	CO6	L4
8	Common Source Amplifier			03	-	1	_	_	1	-	1	C07	L4
9	Comm	on Drain Am	plifier	03	_	1	_	_	1	-	1	C07	L4
10	Differe	ential Amplifi	er	03	-	1	1	_	_	1	1	C07	L4
11	Op-amp			03	-	I	1	_	_	1	1	CO8	L4
12	R-2R DAC			03	_	_	1	_	_	1	1	CO9	L4
13	3 SAR based ADC			03	-	-	_	_	_	-	1	CO10	L4
-		Tota	I	39	5	4	3	5	4	3	13	-	-

Note: Write CO based on the theory course.

2. Continuous Internal Assessment (CIA)

Evaluation	Weightage in Marks	СО	Levels
CIA Exam – 1	15	CO1, CO2, CO3,	L4, L4,L4,L4,L4
		CO4,CO5	
CIA Exam - 2	15	CO6, CO7,	L4,L4
CIA Exam - 3	15	CO8, CO9, CO10	L4, L4, L4
Assignment – 1	05	CO1, CO2, CO3,	L4, L4,L4,L4,L4
		CO4,CO5	
Assignment – 2	05	CO6, CO7,	L4,L4
Assignment – 3	05	CO8, CO9, CO10	L4, L4, L4
Other Activities – define		CO1 to CO10	L4
– Slip test			
Final CIA Marks	0	-	-
_			

SNo	Description	Marks
1	Observation and Weekly Laboratory Activities	04 Marks
2	Record Writing	08 Marks for each Expt
3	Internal Exam Assessment	08 Marks
4	Internal Assessment	20 Marks
5	SEE	80 Marks
-	Total	100 Marks



D. EXPERIMENTS

Experiment 01 :

-	Experiment No.:	1	Marks		Date Planned		Date Conducte	
							d	
1	Title	Inve	rter				1	
2	Course Outcomes	Simu	ulate and sy	nthesize ba	sic VLSI circ	uits using V	erilog codin	g
3	Aim	То и	vrite the ve	rilog code fo	or CMOS In	verter and	write the te	st bench for
		the s	same to vei	rify and obse	erve the wav	eform.		
4	Material /	Lab	Manual					
	Equipment Required							
5	Theory, Formula,	Basi	c structure	of verilog p	programming	g to writing	the verilog p	orogram
	Principle, Concept							
6	Procedure,		 step 1: 	start				
	Program, Activity,	,	 step 2: 	Double clicl	k on Xilinx I	SE 9.2i		
	Algorithm, Pseudo		 step 3: 	File->New	Project.			
	Code		• step 4:	Write the ve	rilog code			
			• step 5:	check Synta:	Χ.			
			• step 6:	if error ther	n correct the	errors		
			• step 7:	Write the Te	est Bench pr	ogram.		
			• Step 8:	Simulate Be	havioral Mo	del		
			• Step 9:	Wave Form	will be displ	ayed		
			• step 10):stop				
7	Block, Circuit,	•	Circuit l	Diagram				
	Model Diagram,	,		vdd				
	Reaction Equation,		F					
	Expected Graph		vin	vout				
			L					
				- gnd				
			Symbol					
			,					
			vin j					
8	Observation Table,	,	Truth T	able				
	Look-up Table,	,	Vin	Vout	•			
	Output		0	1	•			
			1	I V I	•			

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9	9 Sample Calculations -							
10	Graphs	, Outputs		Baseline ▼= 0 Cursor-Baseline ▼= 40ns Name ▼ Baseline ▼ 0 10ns 20ns vin 0 vout 1	TimeA = 40ns 30ns			
11	Results	& Analysis	•	The CMOS Inverter has been successfully simu	lated and verified.			
12	Applica	tion Areas	•	Static RAM, Image sensors				
13	Remark	S						
14	Faculty	Signature	5					
	with Da	te						

Experiment 02 : Buffer

-	Experiment No.:	2	Marks		Date Planned	Date Conducte d				
1	Title	Buffer								
2	Course Outcomes	Simula	te and syr	nthesize bas	ic VLSI circuits u	ising Verilog coding				
3	Aim	To wri	o write the verilog code for CMOS Buffer and write the test bench for the							
		same t	ame to verify and observe the waveform.							
4	Material /	Lab Ma	ab Manual							
	Equipment									
	Required									
5	Theory, Formula,	Formula, Basic structure of verilog programming to writing the verilog program								
	Principle, Concept									
6	Procedure,	•	step 1: s	tart						
	Program, Activity,	•	step 2: E	Double click	on Xilinx ISE 9.2	2i				
	Algorithm, Pseudo	•	step 3: F	ile->New Pi	oject.					
	Code	•	step 4: V	Vrite the ver	ilog code					
		•	step 5:cl	neck Syntax.						
		•	step 6: i	f error then	correct the error	rs				
		•	step 7: V	Vrite the Tes	t Bench progran	n.				
		•	Step 8: S	imulate Beh	avioral Model					
		•	Step 9: V	Vave Form w	vill be displayed					
		•	step 10:	stop						
7	Block, Circuit,	•	Circuit D	iagram						
	Model Diagram,									
	Reaction Equation,		vin	1 2	w 1	vout				
	Expected Graph									

11 IN	AND DE LE CONTROL	SKIT	Teaching Process	Rev No.: 1.0
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			• Symbol	
8	Observa	ation Table,	Truth Table	
	Look-u Output	p Table,	Vin w Vout 0 1 0 1 0 1	
9	Sample Calcula	tions	• -	
10	Graphs	, Outputs	X Image: State of the sta	TimeA = 40ns 30ns
11	Results	& Analysis	The CMOS Buffer has been successfully sim	ulated and verified.
12	Applica	tion Areas	Static RAM, Image sensors	
13	Remark	(S		
14	Faculty with Da	Signature Ite		

Experiment 03 : Transmission Gate

-	Experiment No.:	3	Marks	Date Planned	l Co	Date nducte				
1	Title	Trai	Fransmission Gate							
2	Course Outcomes	Simu	imulate and synthesize basic VLSI circuits using Verilog coding							
3	Aim	То м	To write the verilog code for CMOS Transmission Gate and write the test							
		bend	bench for the same to verify and observe the waveform.							
4	Material /	Lab	Manual							
	Equipment									
	Required									
5	Theory, Formula,	Basic structure of verilog programming to writing the verilog program								
	Principle, Concept									

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RI KRISH		Doc Code:	SKIT.P	5b1.F03		Date:12-08-2018				
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6	Procedu	ure,	•	step 1: start						
	Prograr	n, Activity,	•	step 2: Double click on Xilin	x ISE 9.2i					
	Algoritl	nm, Pseudo	•	step 3: File->New Project.						
	Code		•	step 4: Write the verilog coc	le					
			•	step 5:check Syntax.						
			•	• step 6: if error then correct the errors						
			•	 step 7: Write the Test Bench program. 						
			•	Step 8: Simulate Behavioral	Model					
			•	Step 9: Wave Form will be d	isplayed					
			•	step 10:stop						
7	Block,	Circuit,	• (ircuit Diagram						
	Model	Diagram,		sbar						
	Reactio	n Equation,		in La out						
	Expecte	ed Graph								
				· s						
8	Observ	ation Table,	-	ruth Table						
	Look-u	p Table,								
	Output			s sbar in ou	<u>it</u>					
					2					
					<u> </u>					
9	Sample		• •							
	Calcula	tions								
10	Graphs	. Outputs			e 120ne 130ne	140ne				
		, .								
				- C out 0						
				3 sbar0						
11	Results	& Analvsis	•	he CMOS TG has been succ	essfully simulated a	nd verified.				
12	Applica	tion Areas	• (tatic RAM. Image sensors	· , · · · · · · · · · · · · · · · · · ·					
13	Remark	ς	•							
14	Faculty	Signaturo								
14		Jigilature								

Experiment 04 : Logic Gates

-	Experiment No.:	4	Marks	Date	Date	
				Planned	Conducte	

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1TitleLogic Gates2Course OutcomesSimulate and synthesize Logic gate circuits using Verilog coding3AimTo write the verilog code for CMOS Logic Gates and write the test bench for the same to verify and observe the waveform.4Material Equipment Required/Lab Manual Equipment Required5Theory, Formula, Basic structure of verilog programming to writing the verilog program Principle, Concept- step 1: start6Procedure, Program, Activity, Algorithm, Pseudo Code- step 2: Double click on Xilinx ISE 9.2i - step 3: File->New Project. - step 4: Write the verilog code - step 5: check Syntax. - step 6: if error the arrors - step 6: file ror will be displayed - step 10: stop7Block, Expected Graph- Circuit Diagram - $\frac{a}{b}$ 8Observation Table, Look-up Output- Circuit Table8Observation Table, Look-up Output- Truth Table								d	
2Course OutcomesSimulate and synthesize Logic gate circuits using Verilog coding3AimTo write the verilog code for CMOS Logic Gates and write the test bench for the same to verify and observe the waveform.4Material/Lab ManualEquipment RequiredFormula, Basic structure of verilog programming to writing the verilog program Principle, Concept5Theory, Principle, Concept• step 1: start6Procedure, Program, Activity, Algorithm, Pseudo• step 2: Double click on Xilinx ISE 9.21 Algorithm, Pseudo6Procedure, Principle, Concept• step 3: File->New Project. • step 4: Write the verilog code • step 5: check Syntax. • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10: stop7Block, Circuit, Model Diagram, Reaction Equation, Expected Graph• Circuit Diagram $\frac{a}{b}$ 8Observation Table, OutputTruth Table10 $\frac{a}{b}$ $\frac{a}{b}$ 8Observation Table, 0 Truth Table	1	Title	Logi	c Gates					
3 Aim To write the verilog code for CMOS Logic Gates and write the test bench for the same to verify and observe the waveform. 4 Material /Lab Manual Equipment Required 5 Theory, Formula, Basic structure of verilog programming to writing the verilog program Principle, Concept 6 Procedure, • step 1: start Program, Activity, • step 2: Double click on Xilinx ISE 9.2i Algorithm, Pseudo • step 3: File->New Project. Code • step 4: Write the verilog code • step 5: check Syntax. • step 6: fi error then correct the errors • step 6: fi error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10: stop • Circuit Diagram Reaction Equation, Expected Graph • Circuit Diagram a D = a a D = a = a + b a D = a a D = a = a + b b D = a = a + b a D = a a D = a = a + b b D = a = a + b b D = a = a + b a D = a = a + b a D = a = a + b a D = a = a + b a <th>2</th> <th>Course Outcomes</th> <th>Simu</th> <th>late and sy</th> <th>nthesize Log</th> <th>ic gate circu</th> <th>its using Ve</th> <th>erilog coding</th> <th></th>	2	Course Outcomes	Simu	late and sy	nthesize Log	ic gate circu	its using Ve	erilog coding	
for the same to verify and observe the waveform.4Material/Lab ManualEquipmentRequired5Theory, Formula, Basic structure of verilog programming to writing the verilog program Principle, Concept6Procedure, Program, Activity, Algorithm, Pseudo Code• step 1: start • step 2: Double click on Xilinx ISE 9.21 Algorithm, Pseudo • step 3: File->New Project.Code• step 4: Write the verilog code • step 5: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop7Block, Circuit, • Circuit Diagram Model • Step 4: $a \to b$ • $b \to ce a + b$ • $b \to ce a + b$ • $b \to ce a + b$ 8Observation Table, OutputTruth Table8Observation Table, OutputTruth Table	3	Aim	To w	rite the ver	ilog code fo	r CMOS Log	gic Gates	and write the	e test bench
4 Material /Lab Manual Equipment Required 7 Theory, Formula, Basic structure of verilog programming to writing the verilog program 6 Procedure, • step 1: start 9 Program, Activity, • step 2: Double click on Xilinx ISE 9.2i Algorithm, Pseudo • step 3: File->New Project. Code • step 5: check Syntax. • step 5: check Syntax. • step 6: if error then correct the errors • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10: stop • Circuit Diagram Model Diagram, Reaction Equation, Expected Graph • Circuit Diagram • b • b • b • b • b • b • b • b • b • b • b • b • b • b • b • b • b • b • b • b • b • b • b • b • b • b • b • b • b </th <th></th> <th></th> <th>for t</th> <th>ne same to</th> <th>verify and o</th> <th>oserve the w</th> <th>aveform.</th> <th></th> <th></th>			for t	ne same to	verify and o	oserve the w	aveform.		
Equipment Required5Theory, Formula, Basic structure of verilog programming to writing the verilog program Principle, Concept6Procedure, Program, Activity, Algorithm, Pseudo Code• step 1: start • step 2: Double click on Xilinx ISE 9.2i • step 3: File->New Project. • step 4: Write the verilog code • step 5: check Syntax. • step 5: check Syntax. • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop7Block, Model Diagram, Reaction Equation, Expected Graph• Circuit Diagram b8Observation Table, OutputTruth Table8Observation Table, OutputTruth Table	4	Material /	Lab I	Manual					
RequiredSTheory, Formula, Basic structure of verilog programming to writing the verilog programPrinciple, Concept• step 1: startProgram, Activity, Algorithm, Pseudo Code• step 1: startCode• step 1: start • step 2: Double click on Xilinx ISE 9.2iCode• step 3: File->New Project. • step 5: check Syntax. • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • step 10:stop7Block, Circuit, Model Expected Graph• Circuit Diagram b8Observation Table, OutputTruth Table8Observation Table, OutputTruth Table		Equipment							
5 Theory, Formula, Basic structure of verilog programming to writing the verilog program Principle, Concept • step 1: start 6 Procedure, Program, Activity, • step 1: start Algorithm, Pseudo • step 3: File->New Project. Code • step 4: Write the verilog code • step 5: check Syntax. • step 6: if error then correct the errors • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop • Step 10:stop 7 Block, Circuit, Model Diagram, Reaction Equation, • Circuit Diagram $a \rightarrow b^{D=a + b}$ $a \rightarrow b^{D=a - b^{D}$ $a \rightarrow b^{D=a + b^{D}$ $a \rightarrow b^{D=a + b}$ $a \rightarrow b^{D=a + b^{D}$ $a \rightarrow b^{D=a - b^{D}$ $a \rightarrow b^{D=a + b^{D}$ $a \rightarrow b^{D}$ $b \rightarrow b^{D + D + 1 + 1 + b^{D}$ $a \rightarrow b^{D}$ $b \rightarrow b^{D + 1 + 1 + 1 + b^{D}$ $a \rightarrow b^{D}$ <		Required							
Principle, Concept• step 1: start6Procedure, Program, Activity, Algorithm, Pseudo Code• step 2: Double click on Xilinx ISE 9.2i • step 3: File->New Project. • step 4: Write the verilog code • step 5: check Syntax. • step 5: file->New Project. • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop7Block, Model Diagram, Reaction Equation, Expected Graph• Circuit Diagram a b• Circuit Diagram a b8Observation Table, OutputTruth Table $\frac{a}{b}$ $\frac{1}{b}$ $\frac{1}{b}$ $\frac{1}{b}$ $\frac{1}{b}$ $\frac{1}{b}$ $\frac{1}{b}$ $\frac{1}{b}$	5	Theory, Formula,	Basic	structure of	of verilog pr	ogramming	to writing t	he verilog pr	ogram
6 Procedure, Program, Activity, Algorithm, Pseudo Code code step 3: File->New Project. step 4: Write the verilog code $step 5: check Syntax.step 6: if error then correct the errorsstep 7: Write the Test Bench program.step 8: Simulate Behavioral Modelstep 9: Wave Form will be displayed step 10: stop7 Block, Circuit,Model Diagram,Reaction Equation,Expected Grapha \longrightarrow fi = aba \longrightarrow fi$		Principle, Concept							
Program, Activity, Algorithm, Pseudo• step 3: File -> New Project.Code• step 3: File -> New Project.Code• step 4: Write the verilog code• step 5: check Syntax. • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10: stop7Block, Circuit, • Circuit Diagram • Expected Graph• Circuit Diagram • Circuit Diagram • $a \rightarrow b$ 8Observation Table, OutputTruth Table8Observation Table, 0utputTruth Table	6	Procedure,	•	step 1:	start				
Algorithm, Pseudo: step 3: hle-> New Project.Code: step 4: Write the verilog code: step 5: check Syntax.: step 5: file-> New Project.: step 5: file-> Step Syntax.: step 7: Write the Test Bench program.: Step 8: Simulate Behavioral Model: Step 9: Wave Form will be displayed: Step 10:stop7 Block, Circuit, Model Diagram, Reaction Equation, Expected Graph: Balance : Step 10:stop: Step 2: Step 2: Step 2: Step 3:		Program, Activity,	•	step 2:	Jouble click	on Xilinx ISI	- 9.21		
Code• step 4: Write the Verlig code• step 5:check Syntax.• step 5:check Syntax.• step 5: Write the Test Bench program.• step 7: Write the Test Bench program.• Step 8: Simulate Behavioral Model• Step 9: Wave Form will be displayed• step 10:stop7 Block,Circuit, b• Circuit Diagram Reaction Equation, Expected Graph $a \longrightarrow fi = ab$ b <th></th> <th>Algorithm, Pseudo</th> <th>•</th> <th>step 3:</th> <th>-ile->New Pi</th> <th>roject.</th> <th></th> <th></th> <th></th>		Algorithm, Pseudo	•	step 3:	-ile->New Pi	roject.			
* Step 5: Creck Syntax. • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop 7 Block, Circuit, • Circuit Diagram, Reaction Equation, Expected Graph • b		Code	•	step 4:	write the ver	llog code			
8 Observation Table, Output Truth Table 8 Observation Table, Output Truth Table				step 5:0	f error then	corroct tha			
3 tep 7. Write the rest bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop 7 Block, Circuit, Model Diagram, Reaction Equation, Expected Graph $a \rightarrow b$				step 0.	Nrito tho Tor	t Bonch pro	aram		
8 Observation Table, Output Truth Table 1 $\frac{a}{b}$ $\frac{a}{b}$ $\frac{a}{b}$ $\frac{a}{b}$ 1 $\frac{a}{b}$ $\frac{a}{b}$ $\frac{a}{b}$ $\frac{a}{b}$ $\frac{a}{b}$ $\frac{a}{b}$ $\frac{a}{b}$ $\frac{a}{b}$ $$				Step 7.	Simulate Reh	avioral Mod	al		
$\begin{array}{c} \textbf{a} \textbf{b} \textbf{b} \textbf{c} $				Step 0.	Nave Form w	vill he displa	ved		
7 Block, Circuit, Model Diagram, Reaction Equation, Expected Graph $a \longrightarrow f1 = a b \qquad a \longrightarrow f4 = \overline{a+b}$ $a \longrightarrow f2 = a + b \qquad a \longrightarrow f3 = \overline{a} b$ $a \longrightarrow f3 = \overline{a} \qquad a \longrightarrow f3 = \overline{a} \oplus b$ 8 Observation Table, Look-up Table, Output $b \longrightarrow f3 = \overline{a} \oplus f3 = \overline{a} \oplus b$ $b \longrightarrow f3 = \overline{a} \oplus b$ $b \longrightarrow f3 = \overline{a} \oplus b$ $b \longrightarrow f3 = \overline{a} \oplus b$				step 10	ston		ycu		
7 Block, Circuit, Model Diagram, Reaction Equation, Expected Graph • Circuit Diagram $a \rightarrow b$ $a \rightarrow f1 = ab$ $a \rightarrow f4 = a + b$ $a \rightarrow f2 = a + b$ $a \rightarrow f3 = ab$ $b \rightarrow f2 = a + b$ $a \rightarrow f3 = ab$ $a \rightarrow f3 = a$ $a \rightarrow f3 = ab$ $b \rightarrow f3 = ab$ $a \rightarrow f3 = ab$ $a \rightarrow f3 = a \rightarrow b$ $b \rightarrow f3 = ab$ $a \rightarrow f3 = a \rightarrow b$ $b \rightarrow f3 = ab$ $a \rightarrow f3 = a \rightarrow b$ $b \rightarrow f3 = ab$ $a \rightarrow f3 = a \rightarrow b$ $b \rightarrow f3 = a \oplus b$ 8 Observation Table, Output Truth Table $a \rightarrow f3 = a \rightarrow b$ $a \rightarrow f3 = a \oplus b$				Step 10	stop				
Model Diagram, Reaction Equation, Expected Graph $ \begin{array}{c} a \\ b \\ b \\ \hline b \\ \hline c \\ c \\ c \\ c \\ \hline \hline \hline c \\ \hline \hline \hline c \\ \hline \hline \hline \hline c \\ \hline \hline$	7	Block, Circuit,	•	Circuit D	iagram				
Reaction Equation, $a \\ b \\ column file = ab \\ b \\ column file = ab \\ column fil$		Model Diagram,			5				
Expected Graph a b b b b b b b b b b b b b		Reaction Equation,		a	f1 = a.b	a	f4 = a+b		
$a \longrightarrow f_{2} = a + b \qquad a \longrightarrow f_{3} = \overline{a} b$ $a \longrightarrow f_{3} = \overline{a} \qquad a \longrightarrow f_{3} = \overline{a} \oplus b$ $a \longrightarrow f_{3} = \overline{a} \qquad b \longrightarrow f_{3} = \overline{a} \oplus b$ $a \longrightarrow f_{3} = \overline{a} \oplus b$ $a \longrightarrow f_{3} = \overline{a} \oplus b$ $f_{3} = a$		Expected Graph		Ъ		<u> </u>	<u></u> ,		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$									
$ \begin{array}{c} b \\ b \\ b \\ $				<u>a</u>	f2=a+	·b	f5 = <u>a.b</u>		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$				b	Ð	b			
a $fi = a$ $fi = a \oplus b$ b $fi = a \oplus b$ b $fi = a \oplus b$ 8 Observation Table, Look-up Table, Output Truth Table a $fi = fi =$						a			
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$				a	f3 = a		f6=a⊕b		
8 Observation Table, Look-up Truth Table 0utput Truth Table 0 0 0 1 1 1 0 0 1 0 1 1 1 0						b ⁻ //			
8 Observation Table, Look-up Truth Table 0 0 0 1 1 1 0 1 0 1 1 1 0 0 1 0 1 1 1 1									
8 Observation Table, Look-up Truth Table 0 0 0 1 1 1 0 0 1 0 1 1 1 0 1 0 1 0 1 1 1									
8 Observation Table, Look-up Table, Output Truth Table a b f1 f2 f3 f4 f5 f6 0 0 0 0 1 1 1 0 0 1 0 1 1 1 0									
8 Observation Table, Look-up Truth Table 0 0 0 1 1 1 0 1 0 1 1 1 0 0 1 0 1 1 1 1									
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$									
Look-up Table, Output $a \ b \ f1 \ f2 \ f3 \ f4 \ f5 \ f6 \ 0 \ 0 \ 0 \ 1 \ 1 \ 1 \ 0 \ 0 \ 1 \ 1$	8	Observation Table.		Truth Ta	ble				
Output 0 0 0 1 1 1 0 0 1 0 1 1 1 1 1 1 0 0 1 0 1 1		Look-up Table.			a h	f f2 f3 f4	f5 f6		
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$		Output			0 0	0 0 1 1	1 0		
					0 1	0 1 1 0	1 1		
					1 0	0 1 0 0	1 1		
1 1 1 1 0 0 0 0	L	1	1		1 1	1 1 0 0	0 0		

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9	Sample Calculations	• –
10	Graphs, Outputs	Name Curs 0 10ns 20ns 30ns Image: A construction of the constructi
11	Results & Analysis	 The CMOS Logic gate circuit has been successfully simulated and verified.
12	Application Areas	Alarm switch, Temperature detector, Door bell switch
13	Remarks	
14	Faculty Signature with Date	

Experiment 05 : S-R Flip Flop

-	Experiment No.:	5	Marks	Date	Date	
				Planned	Conducte	,
					d	
1	Title	S-R	Flip flop			
2	Course Outcomes	Simu	ılate and syı	nthesize flip-flop using \	/erilog coding	
3	Aim	To w	rite the ver	ilog code for S-R Flip fl	op and write the test b	ench for the
		same	e to verify a	nd observe the waveform	۱.	
4	Material /	Lab I	Manual			
	Equipment					
	Required					
5	Theory, Formula,	Basic	structure c	of verilog programming	to writing the verilog p	rogram
	Principle, Concept					
6	Procedure,		• step 1: s	start		
	Program, Activity,		• step 2: [Double click on Xilinx ISE	9.2i	
	Algorithm, Pseudo		• step 3: F	ile->New Project.		
	Code		• step 4: V	Vrite the verilog code		
			• step 5:c	heck Syntax.		
		.	• step 6: i	f error then correct the e	rrors	
			• step 7: V	Vrite the Test Bench prog	gram.	

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			• Step) 8: Sim	iulate B	ehavic	oral Model	
			• Step) 9: Wa	ve Form		e displayed	
-		<u> </u>	• step) 10:sto	р			
/	BIOCK,	Circuit,	• Circ	lit Diag	jram			
	Model	Diagram,						
	Reactio	n Equation,	5)		<u>}</u> ♀	
	Expecte	ed Graph	cīk —					
			R-	1)•		Q0	
8	Observ	ation Table.	Trut	h Table	•			
	Look-u	n Table.	Clk		R O ⁺	OЪ	Function	
	Output	p,	1	0 0	Č Č	- Qb	Previous State	
				0 1	1 0	1	Reset	
			I ▲	1 (0 1	0	Set	
			I	1	1 0*	0*	Indataminata	
			1		1 0	0	state	
9	Sample		• –					
	Calcula	tions						
10	Graphs	, Outputs	Name 👻 🛛 🔾	Curs 0		20ns	40ns	60ns 80ns
			🗔 clk 1					
			- 🖸 q 🛛 0					
			🔤 qb 🛛 1					
			- r 1					
			1 3 0					
1 1		0.4	<u> </u>	un d				and the state of the state
	Results	& Analysis	• SK F	lip-flop	o circuit	nas b	een successfully si	mulated and verified.
12	Applica	tion Areas	• Data	storag	e, data	traste	r, registers, counte	ers, trequency division
13	Kemark	.S						
14	Faculty	Signature						
	with Da	ite						

Experiment 06 : D Flip Flop

-	Experiment No.:	6	Marks	Date		Date	
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						d	

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2	Course Outcomes	Simulate and synthesize flip-flop using Verilog coding
3	Aim	To write the verilog code for D Flip flop and write the test bench for the
		same to verify and observe the waveform.
4	Material / Equipment Required	Lab Manual
5	Theory, Formula, Principle, Concept	Basic structure of verilog programming to writing the verilog program
6	Procedure, Program, Activity, Algorithm, Pseudo Code	 step 1: start step 2: Double click on Xilinx ISE 9.2i step 3: File->New Project. step 4: Write the verilog code step 5:check Syntax. step 6: if error then correct the errors step 7: Write the Test Bench program. Step 8: Simulate Behavioral Model Step 9: Wave Form will be displayed step 10:stop
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	 Circuit Diagram Upper provide the second secon
8	Observation Table, Look-up Table, Output	Truth TableclkDQ ⁺ Q ⁺ bFunction \uparrow 001Reset \uparrow 110Set
9	Sample Calculations	• _
10	Graphs, Outputs	Name ▼ C 0 50ns Image: clk 0 Image: clk 0 Image: clk 0 </th

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11	Results	& Analysis	D Flip-flop circuit has been successfully simulate	d and verified.
12	Applica	tion Areas	• Data storage, data trasfer, registers, counters, free	equency division
13	Remark	(S		
14	Faculty	Signature		
	with Da	ite		

Experiment 07 : T Flip Flop

-	Experiment No.:	7	Marks		Date Planned		Date Conducto			
					Flaimeu		d			
1	Title	T Flip	Flip flop							
2	Course Outcomes	Simula	ate and syr	nthesize flip-	-flop using	Verilog codi	ng			
3	Aim	To wr	ite the ver	ilog code fo	r T Flip flo	op and write	e the test be	ench for the		
		same	to verify ar	nd observe t	he waveforn	n.				
4	Material /	Lab M	anual							
	Equipment									
	Required	Desia		£						
5	Principle Concept	Basic	structure o	or verlig pr	ogramming	to writing tr	ie verliog pr	ogram		
6	Procedure.	•	step 1: s	tart						
	Program, Activity,	•	step 2: D	Double click	on Xilinx ISI	E 9.2i				
	Algorithm, Pseudo	•	step 3: F	ile->New Pr	oject.					
	Code	•	step 4: V	Vrite the veri	ilog code					
		•	step 5:cł	neck Syntax.						
		•	step 6: if	f error then	correct the e	errors				
		•	step 7: V	Vrite the Tes	t Bench pro	gram.				
		•	Step 8: S	imulate Beh	avioral Mod	el				
		•	Step 9: V	Vave Form w	vill be displa	yed				
		•	step 10:	stop						
7	Block, Circuit,	•	Circuit D	iagram						
	Model Diagram,									
	Reaction Equation, Expected Graph		T							
			Cik —							
8	Observation Table,		Truth Tal	ble						
	Look-up Table,		clk	T Q [∓] Q [∓] b	Function					
	Output		†	0 Q Qb	Previous state					
Dep	ot		t	1 Qb Q	Toggle					
Prep	pared by						(Checked by		

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9	Sample	• -	
	Calculations		
10	Graphs, Outputs	Name → Cursor → 0	50ns
11	Results & Analysis	• T Flip-flop circuit has been successfully simula	ted and verified.
12	Application Areas	• Data storage, data trasfer, registers, counters,	frequency division
13	Remarks		
14	Faculty Signature		
	with Date		

Experiment 08 : JK Flip Flop

-	Experiment No.:	8	Marks	Date Planned	Date Conducte							
1	Title	JK F	lip flop		d							
2	Course Outcomes	Simu	mulate and synthesize flip-flop using Verilog coding									
3	Aim	To w	rite the ver	ilog code for JK Flip flo	p and write the test be	ench for the						
		same	e to verify a	nd observe the waveform.								
4	Material /	Lab I	b Manual									
	Equipment											
	Required											
5	Theory, Formula,	Basic	structure c	of verilog programming to	o writing the verilog pro	ogram						
	Principle, Concept											
6	Procedure,		step 1: s	start								
	Program, Activity,	•	step 2: [Double click on Xilinx ISE	9.2i							
	Algorithm, Pseudo	•	step 3: F	ile->New Project.								
	Code	•	step 4: V	Vrite the verilog code								
		•	step 5:c	heck Syntax.								
		•	• step 6: i	f error then correct the er	rors							
		•	step 7: V	Write the Test Bench prog	ram.							
		•	Step 8: S	Simulate Behavioral Model	1							
		•	• Step 9: V	wave Form will be displaye	20							
		•	 step 10: 	stop								

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7	Block,	Circuit,	• C	ircui	t D	iagra	m					
	Model	Diagram,		Г				_				
	Reactio	n Equation,))			Q			
	Expecte	ed Graph		Clk —			\geq	$\leq \mid \mid$				
				к —	-)	\square		— Qb			
				L								
8	Observ	ation Table,	Т	ruth	Tal	ble						
	Look-u	p Table,		Clk	J 0	K 0	Q ⁺ O	Q ⁺ Ъ Ob	Function Previous State			
	Output			T 🔺	0	1	0	1	Reset			
				Т •	1	0	1	0	Set			
				4	1	1	Qb	Q	Toggle			
	C											
9	Sample		• –									
1.0	Calcula	tions										
10	Graphs	, Outputs	Name 👻		Curs	0			20ns 40)ns	60ns 80ns	
			clk	0								
			i n	1								
			k 🔤	1						- —		
			P a	1					=			
			db 🔤	_								
	D			(– 1)				-	•	<u> </u>		
11	Results	& Analysis	•]*	. FIIF	D-TI	ор сі	rcuit	: nas	been succes	stully simi	ulated and verified.	
12	Applica	tion Areas	• D	ata s	stor	age,	data	a tra	ster, registers	s, counters	s, frequency division	
13	Remark	(S										
14	Faculty	Signature										
	with Da	ite										

Experiment 09 : Parallel Adder

_	Experiment No.:	9	Marks		Date Planned		Date Conducte d	•	
1	Title	Para	Parallel Adder						
2	Course Outcomes	Simu	Simulate and synthesize adders and counters using Verilog coding						
3	Aim	To v sam	To write the verilog code for parallel adder write the test bench for the same to verify and observe the waveform and synthesize the code.						
4	Material /	Lab	_ab Manual						

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	Equipment	
	Kequirea	Pacie structure of veriles programming to writing the veriles program
5	Principle, Concept	Basic structure of verilog programming to writing the verilog program
6	Procedure,	• step 1: start
	Program, Activity,	 step 2: Double click on Xilinx ISE 9.2i
	Algorithm, Pseudo	 step 3: File->New Project.
	Code	step 4: Write the verilog code
		 step 5:check Syntax.
		 step 6: if error then correct the errors
		 step 7: Write the Test Bench program.
		Step 8: Simulate Behavioral Model
		Step 9: Wave Form will be displayed
		step 10:stop
7	Block, Circuit,	Circuit Diagram
	Model Diagram,	
	Reaction Equation,	B3 A3 B2 A2 B1 A1 B0 A0
	Expected Graph	
		FA4 FA3 FA2 FA2 FA1 FA1
		55 52 51
8	Observation Table,	
	Look-up Table,	
	Output	
	Sample	CASE 1: if A=1001 and B =0011 CASE 2: if A=1001 and B
	Calculations	=0111
		1001 1001
		+ 0011 + 0111
		1100 S3 S2 S1 S0 <u>1</u> 0000
		Cout S3 S2 S1 S0
10	Graphs. Outputs	
	, ,	Traine Curst P Tons 2005 3005 4005
		$\begin{array}{c c c c c c c c c c c c c c c c c c c $
		$\frac{1}{\sqrt{2}} \frac{1}{\sqrt{2}} \frac{1}{\sqrt{2}$
		E C 10 (0 χ3 χο χο
11	Doculto & Analysia	Parallal Adder circuit has been successfully simulated and weified
11	Application Areas	ratanet Auger circuit has been successfully simulated and verified.
12	Application Areas	• Designing ALO, Fast multipliers, Digital clocks, Multiplexing, Parallel

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	J · · · · J · · · ·	
		to serial data conversion
13	Remarks	
14	Faculty Signature	
	with Date	

Experiment 10 : Serial Adder

-	Experiment No.:	10	Marks		Date		Date	
					Planned		Conducte	
1	Titla	Sori	al Adder				a	
2	Course Outcomes	Sim	ilate and svi	nthesize add	ers and cou	nters usina	Verilog codi	na
2	Aim	Том	rite the ver	iloa code fo	r serial add	er write the	test bench	for the same
		to ve	erify and obs	serve the wa	veform and	svnthesize t	he code.	for the sume
4	Material /	Lab	Manual					
	Equipment							
	Required							
5	Theory, Formula,	Basio	c structure c	of verilog pr	ogramming	to writing tl	ne verilog pr	ogram
	Principle, Concept							
6	Procedure,		 step 1: s 	tart				
	Program, Activity,		• step 2: E	Double click	on Xilinx ISE	E 9.2i		
	Algorithm, Pseudo		• step 3: F	ile->New Pr	oject.			
	Code		• step 4: V	Vrite the ver	ilog code			
			 step 5:cl 	heck Syntax.				
			• step 6: i	f error then	correct the e	errors		
			• step 7: v	Vrite the Tes	a Bench pro	gram.		
			 Step 0. 3 Step 0. 1 	Mave Form w	vill be displa	ved		
			• step 10:	stop	nii be displa	yeu		
7	Block. Circuit.	•	Circuit D	iagram				
-	Model Diagram.							
	Reaction Equation.	p	aload shi	8-bit ift reg A	A Full	Sum		8-bit shift reg C
	Expected Graph				B Adder			
						Cout	q -	
				-bit		D-F	Tip Flop	pout
		F	ibload s	hift reg B				
				<u> </u>			hcarry →	
		er	nable					
				• •			•	
						Reset		
Q	Observation Table							
0	Look-up Table							

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	Output	
	Sample	
	Calculations	
10	Graphs, Outputs	Name ▼ Cursor ▼ 0 50ns 100ns 150ns • ▲ data[7:0] 'h 89 xx 89 • ▲ bdata[7:0] 'h 89 xx 89 • ▲ data[7:0] 'h 40 0 0 • ▲ poload 0 0 00 (80(40)(20)(90)(48)(24)(12)(12)(12)(12)(12)(12)(12)(12)(12)(12
11	Results & Analysis	• Serial Adder circuit has been successfully simulated and verified.
12	Application Areas	• Designing ALU, Fast multipilers, Digital clocks, Multiplexing, Parallel to serial data conversion
13	Remarks	
14	Faculty Signature with Date	

Experiment 11 :4-bit Asynchronous Counter

-	Experiment No.:	11	Marks		Date Planned	Date Conducte	
1	Title	Asy	nchronous	Counter		a	
2	Course Outcomes	Simu	late and syr	nthesize add	ers and counter	s using Verilog coding	
3	Aim	To w	rite the ver	ilog code fo	r asynchronous	counter write the test be	ench for
		the s	ame to veri	fy and obser	ve the waveforn	n and synthesize the cod	e.
4	Material /	Lab M	Manual				
	Equipment						
	Required						
5	Theory, Formula,	Basic	structure c	of verilog pr	ogramming to v	riting the verilog progra	m
	Principle, Concept						
6	Procedure,	•	step 1: s	start			
	Program, Activity,	•	step 2: E	Double click	on Xilinx ISE 9.2	li	
	Algorithm, Pseudo	•	step 3: F	ile->New Pr	oject.		
	Code	•	step 4: V	Vrite the ver	ilog code		
		•	step 5:cl	heck Syntax.			
		•	step 6: i	f error then	correct the erro	ſS	
		•	step 7: V	Vrite the Tes	t Bench prograr	n.	
		•	Step 8: S	Simulate Beh	avioral Model		
		•	Step 9: V	Vave Form w	vill be displayed		
		•	step 10:	stop			

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7	Block,	Circuit,	Circuit Diagram	
	Model	Diagram,	Oa Oh C)c Od
	Reactio	n Equation,	logic '1'	
	Expecte	d Graph	T Ta Qa Tb Qb Tc Qc	Td Qd
8	Observa	ation Table,		
	Look-u	p Table,		
	Output			
9	Sample			
	Calcula	tions		
10	Graphs,	Outputs	Name → Cursor 0 50ns 100ns Cursor 0 50ns 100ns Cursor 0 0 0 100ns Cursor 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	150ns
11	Results	& Analysis	 Asynchronous counter circuit has been success verified. 	fully simulated and
12	Applica	tion Areas	 Designing ALU, Fast multipilers, Digital clocks, N to serial data conversion 	Aultiplexing, Parallel
13	Remark	S		
14	Faculty	Signature		
	with Da	te		

Experiment 12 :4-bit synchronous Counter

-	Experiment No.:	12	Marks		Date Planned		Date Conducte	
							d	
1	Title	Syr	Synchronous Counter					
2	Course Outcomes	Simu	Simulate and synthesize adders and counters using Verilog coding					
3	Aim	To v	vrite the ver	ilog code fo	or synchrond	ous counter	write the te	est bench for
		the s	the same to verify and observe the waveform and synthesize the code.					
4	Material /	Lab	Manual					
	Equipment							
	Required							
5	Theory, Formula,	Basi	c structure o	f verilog pr	ogramming	to writing tl	ne verilog pr	ogram
	Principle, Concept							

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0	Procedu	are, Activity	• Step 1: Start							
	Algorith	n, Activity,	Step 2: Double Click on Xilinx ISE 9.21 step 2: File > New Project							
	Algoniti	iiii, Pseudo	 Step 5: File->New Project. step 4: Write the veriles code 							
	Coue		 step 4. Write the verifog code step 5:check Syntax 							
			 step 5.clieck syntax. step 6: if error then correct the errors 							
			 step 0. If error their correct the errors step 7: Write the Test Bench program 							
			Step 7: Write the rest bench program. Step 8: Simulate Behavioral Model							
			Step 9: Wave Form will be displayed							
			 step 10:stop 							
7	Block.	Circuit.	Circuit Diagram							
-	Model	Diagram.								
	Reactio	n Equation.	1	G2						
	Expecte	d Graph								
				Kd						
			Clk							
8	Observa	ation Table,								
	Look-u	p Table,								
	Output									
9	Sample									
	Calcula	tions								
10	Graphs	, Outputs	Name - Cursor 0 50ns 100ns	150ns						
				<u> </u>						
				D [E [F]0]1]2]3						
11	Results	& Analysis	synchronous counter circuit has been success	sfully simulated and						
	Results	a / marysis	verified	indig sinulated and						
12	Applica	tion Areas	Designing ALLI Fast multipilers Digital clocks	Multiplexing Parallel						
12	, ppneu	cion / li cus	to serial data conversion	maniplexing, ruraner						
13	Remark	s								
14	Faculty	Signature								
	with Da	te								

Experiment 13 :CMOS INVERTER

-	Experiment No.:	13	Marks	Date		Date	
				Planne	1	Conducte	

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							d	
1	Title	СМС	S INVERTER	8				
2	Course Outcomes	Desig	gn CMOS In	verter schen	natic , Layou	t and verify	LVS.	
3	Aim	Desi <u>o</u> belov a. Dr i)DC ii)Tra b) Dr	gn an Invert v. aw the sche Analysis. .nsient Anal	er with give ematic and v ysis.	n specification erify the foll	on, completo owing.	e design flov	v mentioned
4	Material / Equipment Required	Lab N	Aanual		y the Dite, E			
5	Theory, Formula, Principle, Concept	Basic	structure c	of CMOS circ	cuits to desig	gn the given	circuit	
6	Procedure, Program, Activity, Algorithm, Pseudo Code	-	step 1: s step 2: [step 3: F step 4: [step 5: 0 step 6: S step 7: 0 Step 8: Step 9: waveforr step 10:	tart Double click Tile->New Draw the circ Check for DR Gave and mir Dpen T-spice File->New Write the Mrite the n	on S-edit cuit C and ERC e nimize e. t-spice cod	errors. e and run	the code,	observe the
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	•	Circuit D	iagram and	Layout diagr	ram	PMOS	

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8	Observation Table, Look-up Table, Output	
9	Sample Calculations	
10	Graphs, Outputs	
11	Results & Analysis	 The schematic and layout for the Inverter is successfully verified and tested.
12	Application Areas	Data converters, Transceivers
13	Remarks	
14	Faculty Signature with Date	

Experiment 14 :Single Stage Differential amplifier

-	Experiment No.:	14	Marks		Date		Date			
					Planned		Conducte			
							d			
1	Title	Sing	le Stage Dif	ferential am	plifier					
2	Course Outcomes	Desi	gn Single Sta	age Differen	tial amplifi	er schematio	: , Layout an	d verify LVS.		
3	Aim	Desi	gn an Sing	le Stage D	Differential	amplifier w	vith given s	specification,		
		com	plete design	flow mentio	oned below.					
		a. Dr	Draw the schematic and verify the following.							
		i)DC	Analysis.							
		ii)AC	Analysis.							
		b) Di	raw the Layo	out and verif	y the DRC, E	ERC				
4	Material /	Lab I	Manual							
	Equipment									
	Required									
5	Theory, Formula,	Basio	structure o	f CMOS cire	cuits to desi	gn the given	circuit			

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	Principl	e, Concept		
6	Procedu	ıre,	• step 1: start	
	Progran	n, Activity,	 step 2: Double click on S-edit 	
	Algorith	ım, Pseudo	 step 3: File->New 	
	Code		• step 4: Draw the circuit	
			• step 5: Check for DRC and ERC errors.	
			• step 6: Save and minimize	
			• step 7: Open T-spice.	
			• Step 8: File->New	
			• Step 9: Write the t-spice code and run th	e code. observe the
			waveform	,
			• step 10:stop	
7	Block	Circuit	Circuit Diagram and Layout diagram	
ľ	Model	Diagram	circuit Diagram and Eayout diagram	
	Peaction	n Equation		
	Evporto	d Craph	царания 1 м.250 Парания на селото н Селото на селото на с	
	Expecte	u Graph	W-25u L-0.603u L-0.603u	
			• Yout	
			₩-2.5u W+2.5u V 10 t=0.66u V V V V V V V V V V V V V V V V V V	
			W-2.Bu V-2.Bu Lia.Au	
			Vref et Vinn y	
			$\begin{pmatrix} +\\ \mathfrak{P}, 8 \end{pmatrix}$ $\begin{pmatrix} +\\ \mathfrak{P}, 1 \end{pmatrix}$ $\begin{pmatrix} +\\ \mathfrak{P}, 1 \end{pmatrix}$	a 4 ⊂
			$\downarrow \forall \downarrow$	Ē
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8 Observation Table, Look-up Table, Output

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9	Sample			
	Calcula	tions		
10	Graphs	, Outputs		
11	Results	& Analysis	 The schematic and layout for the Single stage is successfully verified and tested. 	differential amplifier
12	Applica	tion Areas	• FET, Oscilloscopes, Electronic voltmeters, operat	ional aplifiers
13	Remark	(S		
14	Faculty with Da	Signature Ite		

Experiment 15 :Comon Source Differential amplifier

-	Experiment No.:	15	Marks		Date Planned		Date Conducte	
1	Title	Comm		differential	amplifiar		d	
-	The	Comm	Ion source	e unierential	ampimer			
2	Course Outcomes	Design	n common	source diffe	erential amp	lifier sche	matic , Layo	ut and verify
		LVS.						
3	Aim	Design	n an Com	mon Source	Differential	amplifier	with given s	specification,
		comple	ete design	flow mentio	oned below.			
		a. Drav	w the sche	matic and v	erify the follo	owing.		
		i)DC A	nalysis.					
		ii)AC A	nalysis.					
		b) Drav	w the Layo	out and verif	y the DRC, El	RC		
4	Material /	Lab Ma	anual					
	Equipment							
	Required							
5	Theory, Formula,	Basic s	tructure c	of CMOS circ	uits to desig	n the giver	circuit	
	Principle, Concept							
6	Procedure,	•	step 1: s	tart				
	Program, Activity,	•	step 2: E	Double click	on S–edit			
	Algorithm, Pseudo	•	step 3: F	ile->New				

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	Code		• step 4: Draw the circuit	
			• step 5: Check for DRC and ERC errors.	
			step 6: Save and minimize	
			• step 7: Open T–spice.	
			• Step 8: File->New	
			• Step 9: Write the t-spice code and run the	code, observe the
			waveform	
			• step 10:stop	
	Dia ala	Cincuit	Circuit Diaman del constalia man	
1	BIOCK,	Circuit,	Circuit Diagram and Layout diagram	
	Model	Diagram,	7	
	Evporto	d Craph	Moias de la	
	Expecte	u Graph	W=2.5u	
			L=0.6u	
			W=2.5uW=2.5u 1.0991pF	
			↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	
			L=0.385u	
8	Observa	ation Table,		
	Look-u	p Table,		
	Output			
9	Sample			

Dept Prepared by Approved

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	Calcula	tions		
10	Graphs	, Outputs		
11	Results	& Analysis	 The schematic and layout for the common amplifier is successfully verified and tested. 	source differential
12	Applica	tion Areas	• FET, Oscilloscopes, Electronic voltmeters, operat	ional aplifiers
13	Remark	(S		
14	Faculty	Signature		
	with Da	ite		

Experiment 16 :Comon Drain Differential amplifier

-	Experiment No.:	16	Marks		Date Planned		Date Conducte			
1	Title	Com	mon drain	differential a	amplifier		d			
2	Course Outcomes	Desi <u>o</u> LVS.	esign common drain differential amplifier schematic , Layout and verify VS.							
3	Aim	Desi <u>c</u> comp a. Dr i)DC ii)AC b) Dr	esign an Common Drain Differential amplifier with given specification, omplete design flow mentioned below. Draw the schematic and verify the following. DC Analysis. AC Analysis. Draw the Layout and verify the DBC_EBC							
4	Material / Equipment Required	Lab N	lanual							
5	Theory, Formula, Principle, Concept	Basic	structure c	of CMOS circ	cuits to desig	gn the giver	ı circuit			
6	Procedure, Program, Activity, Algorithm, Pseudo Code	•	step 1: s step 2: [step 3: F step 4: [start Double click File->New Draw the circ	on S–edit :uit					



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11	Results &	& Analysis	 The schematic and layout for the common drain is successfully verified and tested. 	differential amplifier
12	Applicati	on Areas	• FET, Oscilloscopes, Electronic voltmeters, operat	ional aplifiers
13	Remarks			
14	Faculty	Signature		
	with Date	e		

Experiment 17 :R-2R DAC

-	Experiment No.:	17	Marks		Date		Date		
					Planned		Conducte		
							d		
1	Title	R-2	R DAC						
2	Course Outcomes	Desi	gn R-2R DA	C schematic	, Layout an	d verify LVS.			
3	Aim	Desi	gn an R-2	R DAC wit	h given sp	pecification,	complete	design	flow
		men	tioned below	v.					
		a. Dr	raw the sche	matic and v	erify the foll	owing.			
		i)DC	Analysis.						
		ii)AC	Analysis.						
		b) Di	raw the Layo	out and verif	y the DRC, E	RC			
4	Material /	Lab I	Manual						
	Equipment								
	Required								
5	Theory, Formula,	Basio	structure o	f CMOS circ	cuits to desi	gn the given	circuit		
	Principle, Concept								
6	Procedure,		• step 1: s	tart					
	Program, Activity,	.	• step 2: D	Oouble click	on S–edit				
	Algorithm, Pseudo	.	• step 3: F	ile->New					
	Code	.	• step 4: E	Draw the circ	uit				
		.	• step 5: C	Check for DR	C and ERC e	errors.			
		.	• step 6: S	ave and mir	nimize				
		.	• step 7: C	Dpen T-spice	е.				
		.	• Step 8:	File->New					



1 AND	STITUTE OF A	SKIT	Teaching Process	Rev I	Rev No.: 1.0		
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8	ANGALORE	Title:	Course Lab Manual	Page	Page: 37 / 37		
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			and tested.				
12	12 Application Areas		Motor control, digital potentiometers, Se distribution system	oftware	Radio,	Data	
13	Remark	(S					
14	Faculty	Signature					
	with Da	ate					