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Note : Remove "Table of Content" before including in CP Book

15ECL77 : VLSI LAB

A. LABORATORY INFORMATION

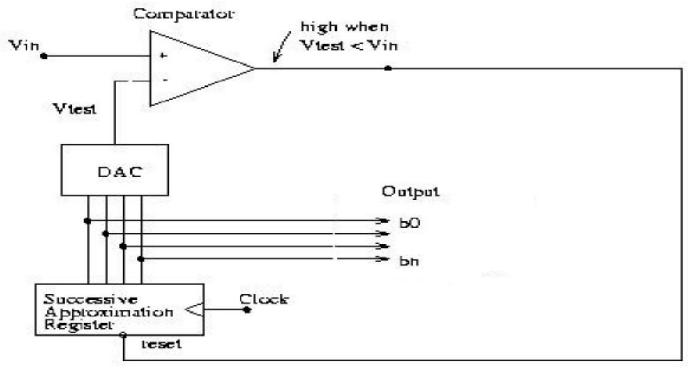
1. Lab Overview

Degree:	B.E	*Program:*	EC
Year / Semester :	4 / 7	*Academic Year:*	2018-19
Course Title:	VLSI Lab	*Course Code:*	15ECL77
Credit / L-T-P:	2 / 0-1-2	*SEE Duration:*	180 Minutes
Total Contact Hours:	40 Hrs	*SEE Marks:*	80 Marks
CIA Marks:	20	*Assignment*	1 / Module
Course Plan Author:	Mrs. Shilpa Rani P	*Sign*	Dt :
Checked By:	Mr.	*Sign*	Dt :

2. Lab Content

Unit	Title of the Experiments	Lab Hours	Concept	Blooms Level
1	Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code i. An inverter ii. A Buffer iii. Transmission Gate	3	Basic VLSI circuits synthesis	L4 Analyze
2	Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code iv. Basic/universal gates	3	Logic Gates synthesis	L4
3	Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code v. Flip flop -RS, D, JK, MS, T	3	Flip-flop synthesis	L4

4	Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code vi. Serial & Parallel adder vii. 4-bit counter [Synchronous and Asynchronous counter]	3	Adders and counters synthesis	L4
5	Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code viii. Successive approximation register [SAR]	3	SAR synthesis	L4
6	Design an Inverter with given specifications**, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) Transient Analysis b. Draw the Layout and verify the DRC, ERC c. Check for LVS d. Extract RC and back annotate the same and verify the Design e. Verify & Optimize for Time, Power and Area to the given constraint*	6	CMOS Inverter design	L4
7	Design the (i) Common source and Common Drain amplifier and (ii) A Single Stage differential amplifier, with given specifications**, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC c. Check for LVS d. Extract RC and back annotate the same and verify the Design.	9	CMOS Aplifiers Design	L4
8	Design an op-amp with given specification** using given differential amplifier Common source and Common Drain amplifier in library*** and completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii). AC Analysis iii) Transient Analysis	3	CMOS OPAMP Design	L4

	b. Draw the Layout and verify the DRC, ERC c. Check for LVS d. Extract RC and back annotate the same and verify the Design.			
9	Design a 4 bit R-2R based DAC for the given specification and completing the design flow mentioned using given op-amp in the library***. a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC	3	R-2R based DAC Design	L4
10	For the SAR based ADC mentioned in the figure below draw the mixed signal schematic and verify the functionality by completing ASIC Design FLOW. [Specifications to GDS-II] 	3	SAR based ADC Design	L4

3. Lab Material

Unit	Details	Available
1	Text books	
	Dept Lab Manual	In Dept Library
2	Reference books	
	1. Digital Logic Applications and Design, John M Yarbrough, Thomson Learning, 2001. ISBN 981-240-062-1.	In College Library
	2. Samir Palnitkar, "**Verilog HDL: A Guide to Digital Design and Synthesis"**, Pearson Education, Second Edition.	In College Library

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	3. **"Basic VLSI Design"**- Douglas A. Pucknell& Kamran Eshraghian, PHI 3rd Edition (original Edition - 1994)	In College Library
3	Others (Web, Video, Simulation, Notes etc.)	

4. Lab Prerequisites:

-	-	Base Course:		-	-
SNo	Course Code	Course Name	Topic / Description	Sem	Remarks
1	15EC33	Digital Elecronics	Logic Gates, Flip-flops, Adders	3	
2	15EC53	Verilog HDL	Gate-Level Modeling,Dataflow Modeling, Behavioral Modeling	5	
3	15EC63	VLSI Design	CMOS circuit Design, Stick diagrams and Layout	6	

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

5. General Instructions

SNo	Instructions	Remarks
1	Observation book and Lab record are compulsory.	
2	Students should report to the concerned lab as per the time table.	
3	After completion of the program, certification of the concerned staff in-charge in the observation book is necessary.	
4	Student should bring a notebook of 100 pages and should enter the readings /observations into the notebook while performing the experiment.	
5	The record of observations along with the detailed experimental procedure of the experiment in the Immediate last session should be submitted and certified staff member in-charge.	
6	Should attempt all experiments given in the list session wise.	
7	It is responsibility to create a separate directory to store all the programs, so that nobody else can read or copy.	
8	When the experiment is completed, should shut down the system properly.	
9	Any damage of the equipment or burn-out components will be viewed seriously either by putting penalty or by dismissing the total group of students from the lab for the semester/year	
10	Completed lab assignments should be submitted in the form of a Lab Record in which you have to write the algorithm, program code along	

	with comments and output for various inputs given	

6. Lab Specific Instructions

SNo	Specific Instructions	Remarks
1	Start computer	
2	Open the text editor	
3	Select new file.	
4	Write the program	
5	Save the program with .v extension.	
6	Compile the program	
7	Execute the program	

B. OBE PARAMETERS

1. Lab / Course Outcomes

#	COs	Teach. Hours	Concept	Instr Method	Assessment Method	Blooms' Level
1	Simulate and synthesize basic VLSI circuits using Verilog coding	3	Basic VLSI circuits synthesis	Demonstration/ Practical	Slip Test	L4
2	Simulate and synthesize logic Gates using Verilog coding	3	Logic Gates synthesis	Practical	Slip Test	L4
3	Simulate and synthesize flip-flops using Verilog coding	3	Flip-flop synthesis	Practical	Slip Test	L4
4	Simulate and synthesize adders and counters using Verilog coding	3	Adders and counters synthesis	Practical	Slip Test	L4
5	Simulate and synthesize SAR using Verilog coding	3	SAR synthesis	Practical	Slip Test	L4
6	Design CMOS Inverter schematic , Layout and verify LVS.	6	CMOS Inverter design	Demonstration/ Practical	Slip Test	L4
7	Design CMOS Amplifier schematic , Layout and verify LVS.	9	CMOS Aplifiers Design	Practical	Slip Test	L4
8	Design Op-amp using differential amplifier and CDA schematic , Layout and verify LVS.	3	CMOS OPAMP Design	Practical	Slip Test	L4
9	Design R-2R DAC schematic, Layout	3	R-2R based	Practica	Slip Test	L4

	and verify DRC, ERC		DAC Design	l		
10	Draw mixed signal schematic and verify its functionality of SAR based ADC	3	SAR based ADC Design	Practical	Slip Test	L4
-	**Total**	**39**	-	-	-	-

Note: Identify a max of 2 Concepts per unit. Write 1 CO per concept.

2. Lab Applications

SNo	Application Area	CO	Level
1	Static RAM, Image sensors	CO1	L4
2	Alarm switch, Temperature detector, Door bell switch	CO2	L4
3	Data storage, data trasfer, registers, counters, frequency division	CO3	L4
4	Designing ALU, Fast multipilers, Digital clocks, Multiplexing, Parallel to serial data conversion	CO4	L4
5	Analog to digital conversion, PLC application	CO5	L4
6	Data converters, Transceivers	CO6	L4
7	FET, Oscilloscopes, Electronic voltmeters, operational aplifiers	CO7	L4
8	Voltage summer, Integrators, digital to analog connversion	CO8	L4
9	Motor control, digital potentiometers, Software Radio, Data distribution system	CO9	L4
10	Temperature sensors, bus architecture in microcontroller, distance locator	CO10	L4

Note: Write 1 or 2 applications per CO.

3. Articulation Matrix

(CO – PO MAPPING)

-	Course Outcomes	Program Outcomes											
#	COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	Level
15ECL77.1	Simulate and synthesize basic VLSI circuits using Verilog coding	3	1			3				3				L4
15ECL77.2	Simulate and synthesize logic Gates using Verilog coding	3	1			3				3				L4
15ECL77.3	Simulate and synthesize flip-flops using Verilog coding	3	1			3				3				L4
15ECL77.4	Simulate and synthesize adders and counters using Verilog coding	3	1			3				3				L4
15ECL77.5	Simulate and synthesize SAR	3	1			3				3				L4

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	using Verilog coding													
15ECL77.6	Design CMOS Inverter schematic , Layout and verify LVS.	3	2	1		3				3				L4
15ECL77.7	Design CMOS Amplifier schematic , Layout and verify LVS.	3	2	1		3				3				L4
15ECL77.8	Design Op-amp using differential amplifier and CDA schematic , Layout and verify LVS.	3	2	1		3				3				L4
15ECL77.9	Design R-2R DAC schematic, Layout and verify DRC, ERC	3	2	1		3				3				L4
15ECL77.10	Draw mixed signal schematic and verify its functionality of SAR based ADC	3	2	1		3				3				L4
	Average	**3**	**1.5**	**0.5**		**3**				**3**				

Note: Mention the mapping strength as 1, 2, or 3

4. Mapping Justification

Mapping		Mapping Level	Justification
CO	**PO**	**-**	**-**
CO1	PO1	3	Knowledge of basic VLSI circuits is required for understanding complex VLSI problems
CO1	PO2	1	Knowledge of basic VLSI circuits is required for problem analysis in VLSI designs.
CO1	PO5	3	Simulation of basic VLSI circuits requires tools like “xilinx”
CO1	PO9	1	Individual and team work is required for simulation of basic VLSI circuits.
CO2	PO1	3	Knowledge of logic gates is required for understanding complex VLSI problems
CO2	PO2	1	Knowledge of logic gates is required for problem analysis in VLSI designs.
CO2	PO5	3	Simulation of logic gate circuits requires tools like “xilinx”
CO2	PO9	1	Individual and team work is required for simulation of logic gates.
CO3	PO1	3	Knowledge of flip-flops is required for understanding complex VLSI problems
CO3	PO2	1	Knowledge of flip-flops is required for problem analysis in VLSI designs.
CO3	PO5	3	Simulation of flip-flop circuits requires tools like “xilinx”
CO3	PO9	1	Individual and team work is required for simulation of Flip-flops

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CO4	PO1	3	Knowledge of adders is required for understanding complex VLSI problems
CO4	PO2	1	Knowledge of adders is required for problem analysis in VLSI designs.
CO4	PO5	3	Simulation of adder circuits requires tools like “xilinx”
CO4	PO9	1	Individual and team work is required for simulation of adders
CO5	PO1	3	Knowledge of SAR is required for understanding analog to digital convertion
CO5	PO2	1	Knowledge of SAR is required for problem analysis in VLSI designs.
CO5	PO5	3	Simulation of SAR circuit requires tools like “xilinx”
CO5	PO9	1	Individual and team work is required for simulation of SAR
CO6	PO1	3	Knowledge of CMOS Inverter is required for understanding complex VLSI problems
CO6	PO2	2	Knowledge of CMOS Inverter is required for problem analysis in VLSI designs.
CO6	PO3	1	Designing of CMOS Inverter is required for development of complex VLSI circuits
CO6	PO5	3	Design of CMOS Inverter requires “cadence” or “tanner tools” usage.
CO6	PO9	2	Individual and team work is required for design of CMOS Inverter
CO7	PO1	3	Knowledge of CMOS Amplifiers is required for solution of amplification related problems
CO7	PO2	2	Knowledge of CMOS Amplifiers is required for problem analysis in VLSI designs.
CO7	PO3	1	Designing of CMOS Amplifiers is required for development of complex VLSI circuits
CO7	PO5	3	Design of CMOS Amplifiers requires “cadence” or “tanner tools” usage.
CO7	PO9	2	Individual and team work is required for design of CMOS Amplifiers
CO8	PO1	3	Knowledge of Op-amp is required for solution of amplification related problems
CO8	PO2	2	Knowledge of Op-amp is required for problem analysis in VLSI designs.
CO8	PO3	1	Designing of Op-amp is required for development of complex VLSI circuits
CO8	PO5	3	Design of Op-amp requires “cadence” or “tanner tools” usage.
CO8	PO9	2	Individual and team work is required for design of Op-amp
CO9	PO1	3	Knowledge of DAC is required for solving signal conversion related problems
CO9	PO2	2	Knowledge of DAC is required for problem analysis in VLSI designs.
CO9	PO3	1	Designing of DAC is required for development of complex VLSI circuits
CO9	PO5	3	Design of DAC requires “cadence” or “tanner tools” usage.
CO9	PO9	2	Individual and team work is required for design of DAC

CO10	PO1	3	Knowledge of SAR is required for solving signal conversion related problems
CO10	PO2	2	Knowledge of SAR is required for problem analysis in VLSI designs.
CO10	PO3	1	Designing of SAR is required for development of complex VLSI circuits
CO10	PO5	3	Design of SAR requires “cadence” or “tanner tools” usage.
CO10	PO9	2	Individual and team work is required for design of SAR

Note: Write justification for each CO-PO mapping.

5. Curricular Gap and Content

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					

Note: Write Gap topics from A.4 and add others also.

6. Content Beyond Syllabus

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					

Note: Anything not covered above is included here.

C. COURSE ASSESSMENT

1. Course Coverage

Unit	Title	Teaching Hours	No. of question in Exam							CO	Levels
			CIA-1	CIA-2	CIA-3	Asg-1	Asg-2	Asg-3	SEE		
1	Inverter, Buffer, TG	03	1	–	–	1	–	–	1	CO1	L4
2	Logic gates	03	1	–	–	1	–	–	1	CO2	L4
3	Flip-flops	03	1	–	–	1	–	–	1	CO3	L4
4	Adders, Counters	03	1	–	–	1	–	–	1	CO4	L4
5	SAR	03	1	–	–	1	–	–	1	CO5	L4

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6	CMOS Inverter Schematic	03	–	1	–	–	1	–	1	CO6	L4
7	CMOS Inverter Layout	03	–	1	–	–	1	–	1	CO6	L4
8	Common Source Amplifier	03	–	1	–	–	1	–	1	CO7	L4
9	Common Drain Amplifier	03	–	1	–	–	1	–	1	CO7	L4
10	Differential Amplifier	03	–	–	1	–	–	1	1	CO7	L4
11	Op-amp	03	–	–	1	–	–	1	1	CO8	L4
12	R-2R DAC	03	–	–	1	–	–	1	1	CO9	L4
13	SAR based ADC	03	–	–	–	–	–	–	1	CO10	L4
-	**Total**	**39**	**5**	**4**	**3**	**5**	**4**	**3**	**13**	**-**	**-**

Note: Write CO based on the theory course.

2. Continuous Internal Assessment (CIA)

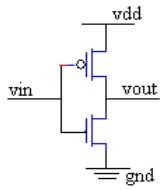
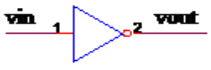
Evaluation	Weightage in Marks	CO	Levels
CIA Exam – 1	15	CO1, CO2, CO3, CO4,CO5	L4, L4,L4,L4,L4
CIA Exam – 2	15	CO6, CO7,	L4,L4
CIA Exam – 3	15	CO8, CO9, CO10	L4, L4, L4
Assignment – 1	05	CO1, CO2, CO3, CO4,CO5	L4, L4,L4,L4,L4
Assignment – 2	05	CO6, CO7,	L4,L4
Assignment – 3	05	CO8, CO9, CO10	L4, L4, L4
Other Activities – define – Slip test		CO1 to CO10	L4
Final CIA Marks	**0**	**-**	**-**

–

SNo	Description	Marks
1	Observation and Weekly Laboratory Activities	04 Marks
2	Record Writing	08 Marks for each Expt
3	Internal Exam Assessment	08 Marks
4	Internal Assessment	20 Marks
5	SEE	80 Marks
-	**Total**	**100 Marks**

D. EXPERIMENTS

Experiment 01 :

-	**Experiment No.:**	1	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Inverter						
2	Course Outcomes	Simulate and synthesize basic VLSI circuits using Verilog coding						
3	Aim	To write the verilog code for **CMOS Inverter** and write the test bench for the same to verify and observe the waveform.						
4	Material / Equipment Required	Lab Manual						
5	Theory, Formula, Principle, Concept	Basic structure of verilog programming to writing the verilog program						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• step 1: start • step 2: Double click on Xilinx ISE 9.2i • step 3: File->New Project. • step 4: Write the verilog code • step 5:check Syntax. • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram  • Symbol  						
8	Observation Table, Look-up Table, Output	Truth Table •						

Vin	Vout
0	1
1	0

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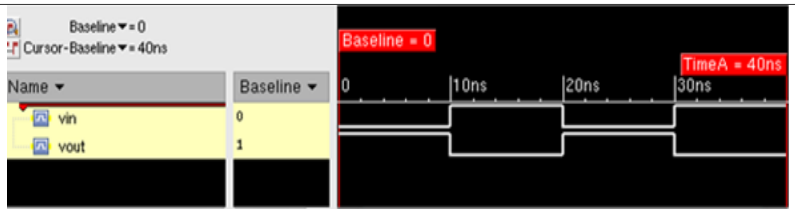
9	Sample Calculations	• –
10	Graphs, Outputs	
11	Results & Analysis	• The CMOS Inverter has been successfully simulated and verified.
12	Application Areas	• Static RAM, Image sensors
13	Remarks	
14	Faculty Signature with Date	

Experiment 02 : Buffer

–	**Experiment No.:**	2	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Buffer						
2	Course Outcomes	Simulate and synthesize basic VLSI circuits using Verilog coding						
3	Aim	To write the verilog code for **CMOS Buffer** and write the test bench for the same to verify and observe the waveform.						
4	Material / Equipment Required	Lab Manual						
5	Theory, Formula, Principle, Concept	Basic structure of verilog programming to writing the verilog program						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• step 1: start • step 2: Double click on Xilinx ISE 9.2i • step 3: File->New Project. • step 4: Write the verilog code • step 5:check Syntax. • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram 						

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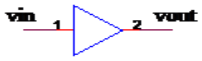
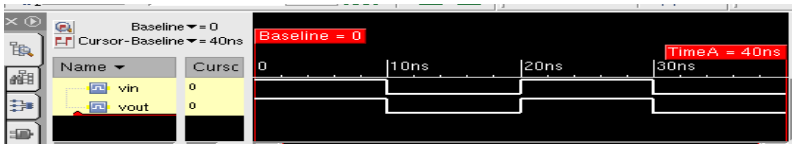
		• Symbol 
8	Observation Table, Look-up Table, Output	Truth Table Vin | w | Vout 0 | 1 | 0 1 | 0 | 1
9	Sample Calculations	• –
10	Graphs, Outputs	
11	Results & Analysis	• The CMOS Buffer has been successfully simulated and verified.
12	Application Areas	• Static RAM, Image sensors
13	Remarks	
14	Faculty Signature with Date	

Experiment 03 : Transmission Gate

–	**Experiment No.:**	3	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Transmission Gate						
2	Course Outcomes	Simulate and synthesize basic VLSI circuits using Verilog coding						
3	Aim	To write the verilog code for **CMOS Transmission Gate** and write the test bench for the same to verify and observe the waveform.						
4	Material / Equipment Required	Lab Manual						
5	Theory, Formula, Principle, Concept	Basic structure of verilog programming to writing the verilog program						

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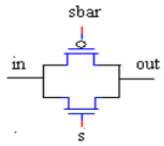
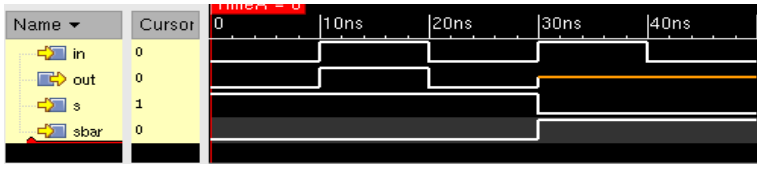
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• step 1: start • step 2: Double click on Xilinx ISE 9.2i • step 3: File->New Project. • step 4: Write the verilog code • step 5:check Syntax. • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram 
8	Observation Table, Look-up Table, Output	Truth Table s | sbar | in | out 1 | 0 | 0 | 0 1 | 0 | 1 | 1 0 | 1 | 0 | z 0 | 1 | 1 | z
9	Sample Calculations	• -
10	Graphs, Outputs	
11	Results & Analysis	• The CMOS TG has been successfully simulated and verified.
12	Application Areas	• Static RAM, Image sensors
13	Remarks	
14	Faculty Signature with Date	

Experiment 04 : Logic Gates

-	**Experiment No.:**	4	**Marks**		**Date Planned**		**Date Conducte**	

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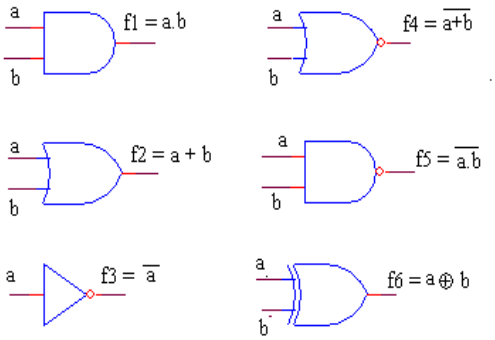
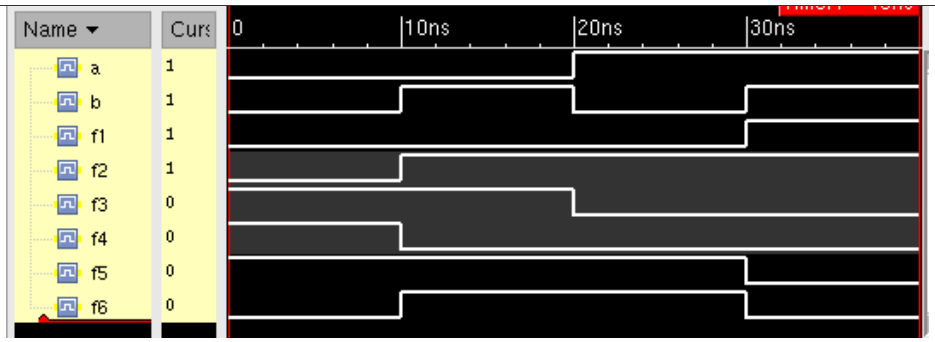
1	Title	Logic Gates
2	Course Outcomes	Simulate and synthesize Logic gate circuits using Verilog coding
3	Aim	To write the verilog code for **CMOS Logic Gates** and write the test bench for the same to verify and observe the waveform.
4	Material / Equipment Required	Lab Manual
5	Theory, Formula, Principle, Concept	Basic structure of verilog programming to writing the verilog program
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• step 1: start • step 2: Double click on Xilinx ISE 9.2i • step 3: File->New Project. • step 4: Write the verilog code • step 5:check Syntax. • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram 
8	Observation Table, Look-up Table, Output	Truth Table

a	b	f1	f2	f3	f4	f5	f6
0	0	0	0	1	1	1	0
0	1	0	1	1	0	1	1
1	0	0	1	0	0	1	1
1	1	1	1	0	0	0	0

9	Sample Calculations	• –
10	Graphs, Outputs	
11	Results & Analysis	• The CMOS Logic gate circuit has been successfully simulated and verified.
12	Application Areas	• Alarm switch, Temperature detector, Door bell switch
13	Remarks	
14	Faculty Signature with Date	

Experiment 05 : S-R Flip Flop

–	**Experiment No.:**	5	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	S-R Flip flop						
2	Course Outcomes	Simulate and synthesize flip-flop using Verilog coding						
3	Aim	To write the verilog code for **S-R Flip flop** and write the test bench for the same to verify and observe the waveform.						
4	Material / Equipment Required	Lab Manual						
5	Theory, Formula, Principle, Concept	Basic structure of verilog programming to writing the verilog program						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• step 1: start • step 2: Double click on Xilinx ISE 9.2i • step 3: File->New Project. • step 4: Write the verilog code • step 5:check Syntax. • step 6: if error then correct the errors • step 7: Write the Test Bench program.						

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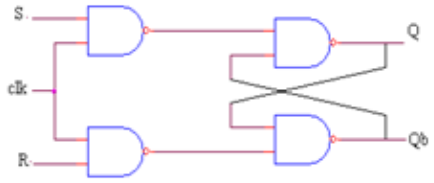
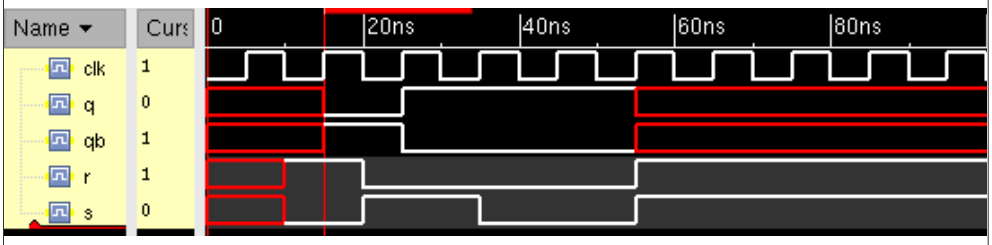
		• Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram 
8	Observation Table, Look-up Table, Output	Truth Table **Clk** | **S** | **R** | **Q⁺** | **Q⁺b** | **Function** ↑ | 0 | 0 | Q | Qb | Previous State ↑ | 0 | 1 | 0 | 1 | Reset ↑ | 1 | 0 | 1 | 0 | Set ↑ | 1 | 1 | 0* | 0* | Indeterminate state
9	Sample Calculations	• –
10	Graphs, Outputs	
11	Results & Analysis	• SR Flip-flop circuit has been successfully simulated and verified.
12	Application Areas	• Data storage, data trasfer, registers, counters, frequency division
13	Remarks	
14	Faculty Signature with Date	

Experiment 06 : D Flip Flop

–	**Experiment No.:**	6	**Marks**		**Date Planned**		**Date Conducted**	

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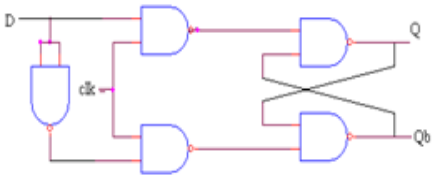
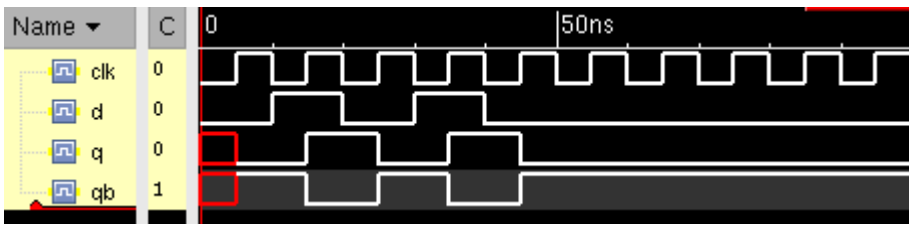
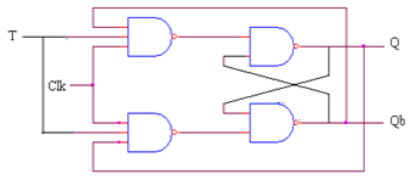
1	Title	D Flip flop
2	Course Outcomes	Simulate and synthesize flip-flop using Verilog coding
3	Aim	To write the verilog code for **D Flip flop** and write the test bench for the same to verify and observe the waveform.
4	Material / Equipment Required	Lab Manual
5	Theory, Formula, Principle, Concept	Basic structure of verilog programming to writing the verilog program
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• step 1: start • step 2: Double click on Xilinx ISE 9.2i • step 3: File->New Project. • step 4: Write the verilog code • step 5:check Syntax. • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram 
8	Observation Table, Look-up Table, Output	Truth Table clk | D | Q^+ | Q^+b | Function ↑ | 0 | 0 | 1 | Reset ↑ | 1 | 1 | 0 | Set
9	Sample Calculations	• -
10	Graphs, Outputs	

11	Results & Analysis	• D Flip-flop circuit has been successfully simulated and verified.
12	Application Areas	• Data storage, data trasfer, registers, counters, frequency division
13	Remarks	
14	Faculty Signature with Date	

Experiment 07 : T Flip Flop

-	**Experiment No.:**	7	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	T Flip flop						
2	Course Outcomes	Simulate and synthesize flip-flop using Verilog coding						
3	Aim	To write the verilog code for **T Flip flop** and write the test bench for the same to verify and observe the waveform.						
4	Material / Equipment Required	Lab Manual						
5	Theory, Formula, Principle, Concept	Basic structure of verilog programming to writing the verilog program						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• step 1: start • step 2: Double click on Xilinx ISE 9.2i • step 3: File->New Project. • step 4: Write the verilog code • step 5:check Syntax. • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram 						
8	Observation Table, Look-up Table, Output	Truth Table clk | T | Q+ | Q+b | Function ↑ | 0 | Q | Qb | Previous state ↑ | 1 | Qb | Q | Toggle						

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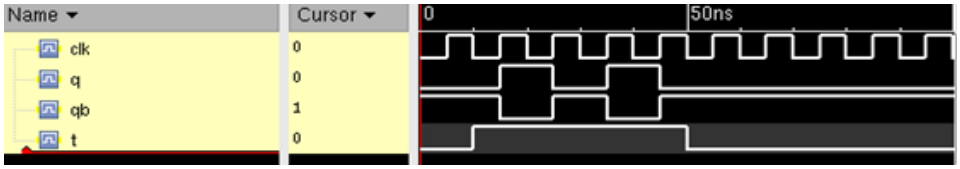
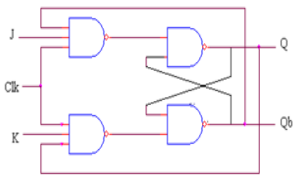
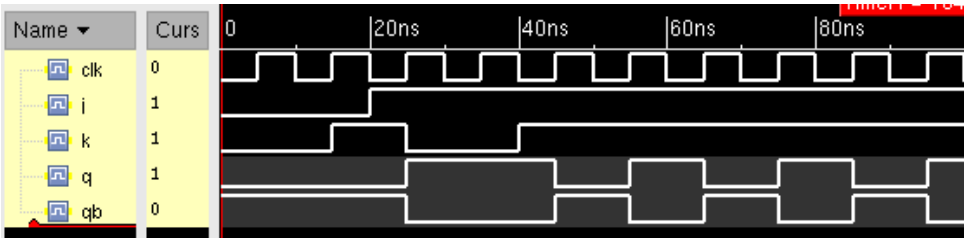
9	Sample Calculations	• –
10	Graphs, Outputs	
11	Results & Analysis	• T Flip-flop circuit has been successfully simulated and verified.
12	Application Areas	• Data storage, data trasfer, registers, counters, frequency division
13	Remarks	
14	Faculty Signature with Date	

Experiment 08 : JK Flip Flop

–	**Experiment No.:**	8	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	JK Flip flop						
2	Course Outcomes	Simulate and synthesize flip-flop using Verilog coding						
3	Aim	To write the verilog code for **JK Flip flop** and write the test bench for the same to verify and observe the waveform.						
4	Material / Equipment Required	Lab Manual						
5	Theory, Formula, Principle, Concept	Basic structure of verilog programming to writing the verilog program						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• step 1: start • step 2: Double click on Xilinx ISE 9.2i • step 3: File->New Project. • step 4: Write the verilog code • step 5:check Syntax. • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop						

7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram 
8	Observation Table, Look-up Table, Output	Truth Table Clk J K Q^+ Q^+b Function ↑ 0 0 Q Qb Previous State ↑ 0 1 0 1 Reset ↑ 1 0 1 0 Set ↑ 1 1 Qb Q Toggle
9	Sample Calculations	• –
10	Graphs, Outputs	
11	Results & Analysis	• JK Flip-flop circuit has been successfully simulated and verified.
12	Application Areas	• Data storage, data trasfer, registers, counters, frequency division
13	Remarks	
14	Faculty Signature with Date	

Experiment 09 : Parallel Adder

–	**Experiment No.:**	9	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Parallel Adder						
2	Course Outcomes	Simulate and synthesize adders and counters using Verilog coding						
3	Aim	To write the verilog code for parallel adder write the test bench for the same to verify and observe the waveform and synthesize the code.						
4	Material /	Lab Manual						

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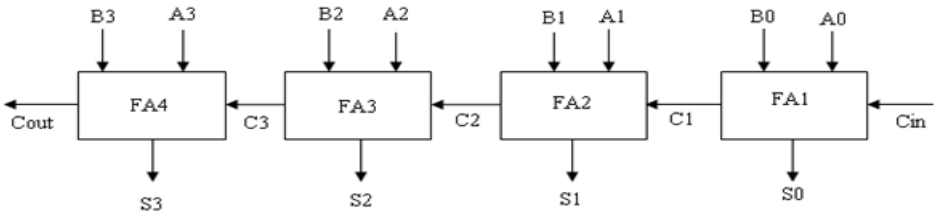
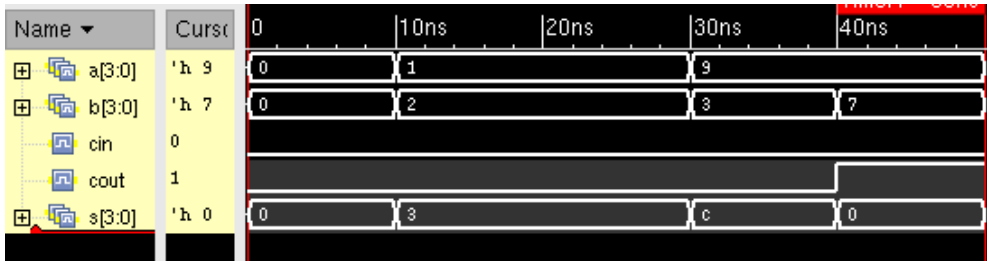
	Equipment Required	
5	Theory, Formula, Principle, Concept	Basic structure of verilog programming to writing the verilog program
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• step 1: start • step 2: Double click on Xilinx ISE 9.2i • step 3: File->New Project. • step 4: Write the verilog code • step 5:check Syntax. • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram 
8	Observation Table, Look-up Table, Output	
	Sample Calculations	**CASE 1: if A=1001 and B =0011 CASE 2: if A=1001 and B =0111** **1001 1001** **+ 0011 + 0111** **1100 S3 S2 S1 S0 1 0000** **Cout S3 S2 S1 S0**
10	Graphs, Outputs	
11	Results & Analysis	• Parallel Adder circuit has been successfully simulated and verified.
12	Application Areas	• Designing ALU, Fast multipilers, Digital clocks, Multiplexing, Parallel

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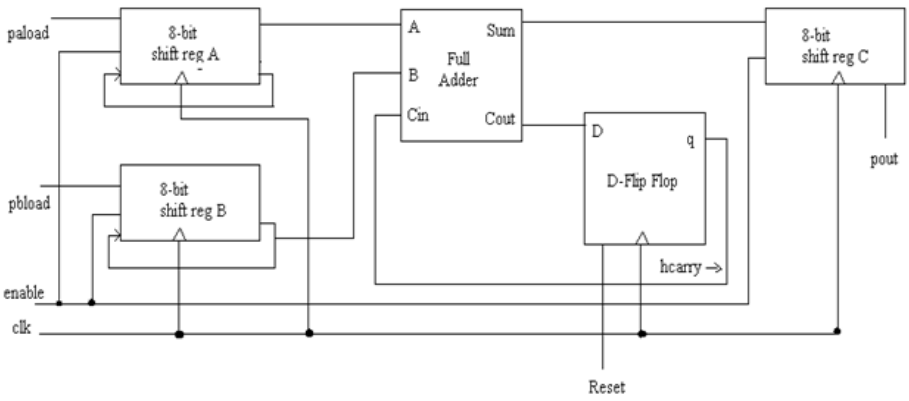
		to serial data conversion
13	Remarks	
14	Faculty Signature with Date	

Experiment 10 : Serial Adder

-	**Experiment No.:**	10	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Serial Adder						
2	Course Outcomes	Simulate and synthesize adders and counters using Verilog coding						
3	Aim	To write the verilog code for serial adder write the test bench for the same to verify and observe the waveform and synthesize the code.						
4	Material / Equipment Required	Lab Manual						
5	Theory, Formula, Principle, Concept	Basic structure of verilog programming to writing the verilog program						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• step 1: start • step 2: Double click on Xilinx ISE 9.2i • step 3: File->New Project. • step 4: Write the verilog code • step 5:check Syntax. • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram 						
8	Observation Table, Look-up Table,							

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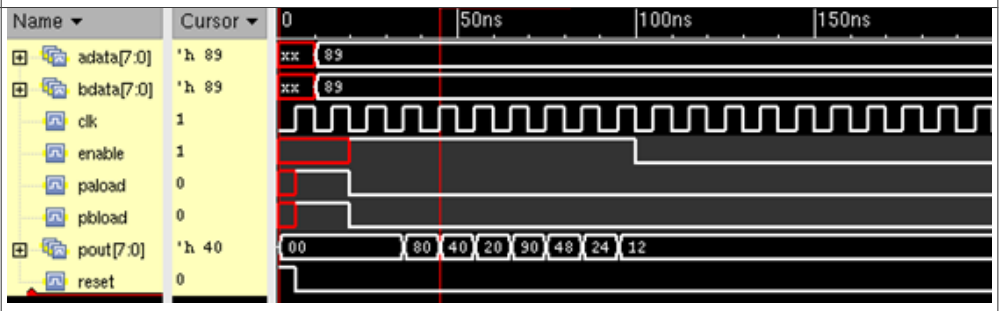
	Output	
	Sample Calculations	
10	Graphs, Outputs	
11	Results & Analysis	• Serial Adder circuit has been successfully simulated and verified.
12	Application Areas	• Designing ALU, Fast multipilers, Digital clocks, Multiplexing, Parallel to serial data conversion
13	Remarks	
14	Faculty Signature with Date	

Experiment 11 :4-bit Asynchronous Counter

-	**Experiment No.:**	11	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Asynchronous Counter						
2	Course Outcomes	Simulate and synthesize adders and counters using Verilog coding						
3	Aim	To write the verilog code for asynchronous counter write the test bench for the same to verify and observe the waveform and synthesize the code.						
4	Material / Equipment Required	Lab Manual						
5	Theory, Formula, Principle, Concept	Basic structure of verilog programming to writing the verilog program						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• step 1: start • step 2: Double click on Xilinx ISE 9.2i • step 3: File->New Project. • step 4: Write the verilog code • step 5:check Syntax. • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop						

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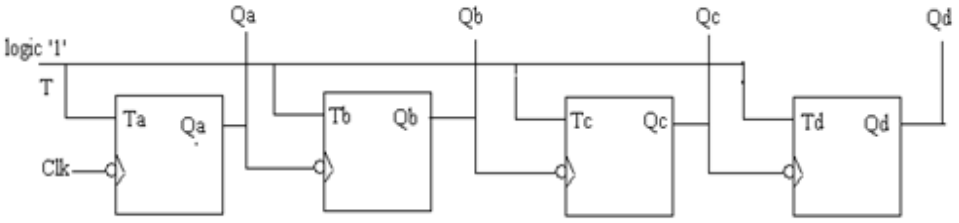
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram 
8	Observation Table, Look-up Table, Output	
9	Sample Calculations	
10	Graphs, Outputs	
11	Results & Analysis	• Asynchronous counter circuit has been successfully simulated and verified.
12	Application Areas	• Designing ALU, Fast multipilers, Digital clocks, Multiplexing, Parallel to serial data conversion
13	Remarks	
14	Faculty Signature with Date	

Experiment 12 :4-bit synchronous Counter

-	**Experiment No.:**	12	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Synchronous Counter						
2	Course Outcomes	Simulate and synthesize adders and counters using Verilog coding						
3	Aim	To write the verilog code for synchronous counter write the test bench for the same to verify and observe the waveform and synthesize the code.						
4	Material / Equipment Required	Lab Manual						
5	Theory, Formula, Principle, Concept	Basic structure of verilog programming to writing the verilog program						

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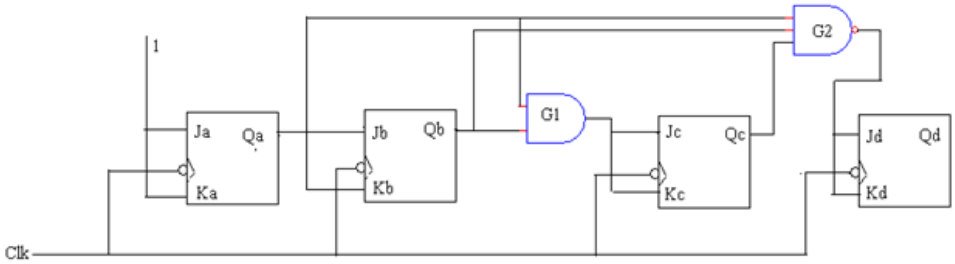
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• step 1: start • step 2: Double click on Xilinx ISE 9.2i • step 3: File->New Project. • step 4: Write the verilog code • step 5:check Syntax. • step 6: if error then correct the errors • step 7: Write the Test Bench program. • Step 8: Simulate Behavioral Model • Step 9: Wave Form will be displayed • step 10:stop
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram 
8	Observation Table, Look-up Table, Output	
9	Sample Calculations	
10	Graphs, Outputs	
11	Results & Analysis	• synchronous counter circuit has been successfully simulated and verified.
12	Application Areas	• Designing ALU, Fast multipilers, Digital clocks, Multiplexing, Parallel to serial data conversion
13	Remarks	
14	Faculty Signature with Date	

Experiment 13 :CMOS INVERTER

-	**Experiment No.:**	13	**Marks**		**Date Planned**		**Date Conducte**	

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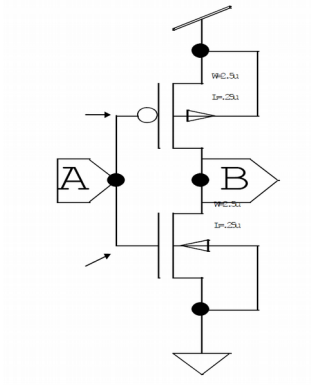
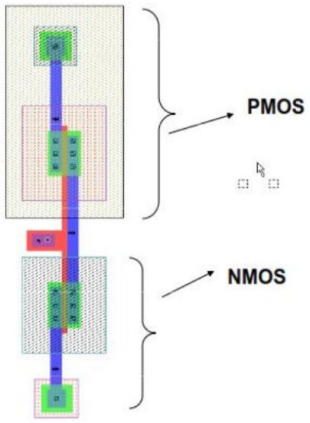
							d	
1	Title	CMOS INVERTER						
2	Course Outcomes	Design CMOS Inverter schematic , Layout and verify LVS.						
3	Aim	Design an Inverter with given specification, complete design flow mentioned below. a. Draw the schematic and verify the following. i)DC Analysis. ii)Transient Analysis. b) Draw the Layout and verify the DRC, ERC						
4	Material / Equipment Required	Lab Manual						
5	Theory, Formula, Principle, Concept	Basic structure of CMOS circuits to design the given circuit						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• step 1: start • step 2: Double click on S-edit • step 3: File->New • step 4: Draw the circuit • step 5: Check for DRC and ERC errors. • step 6: Save and minimize • step 7: Open T-spice. • Step 8: File->New • Step 9: Write the t-spice code and run the code, observe the waveform • step 10:stop						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram and Layout diagram  						

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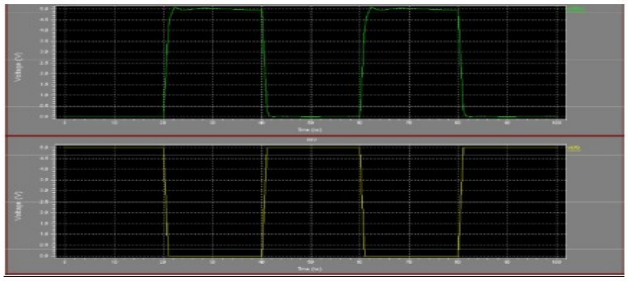
8	Observation Table, Look-up Table, Output	
9	Sample Calculations	
10	Graphs, Outputs	
11	Results & Analysis	• The schematic and layout for the Inverter is successfully verified and tested.
12	Application Areas	• Data converters, Transceivers
13	Remarks	
14	Faculty Signature with Date	

Experiment 14 :Single Stage Differential amplifier

-	**Experiment No.:**	14	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Single Stage Differential amplifier						
2	Course Outcomes	Design Single Stage Differential amplifier schematic , Layout and verify LVS.						
3	Aim	Design an Single Stage Differential amplifier with given specification, complete design flow mentioned below. a. Draw the schematic and verify the following. i)DC Analysis. ii)AC Analysis. b) Draw the Layout and verify the DRC, ERC						
4	Material / Equipment Required	Lab Manual						
5	Theory, Formula,	Basic structure of CMOS circuits to design the given circuit						

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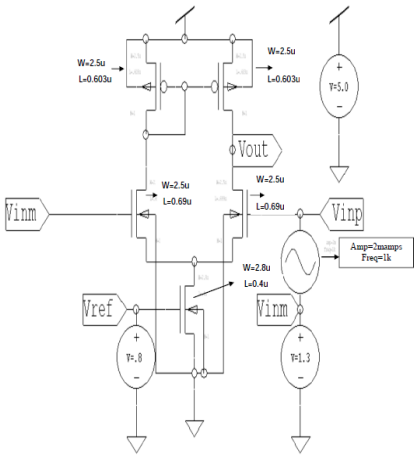
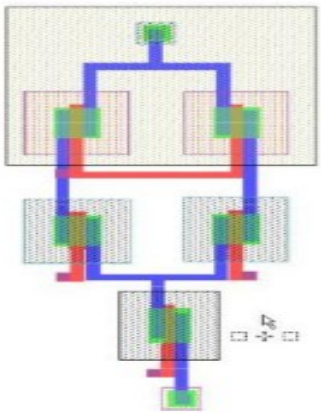
	Principle, Concept	
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• step 1: start • step 2: Double click on S-edit • step 3: File->New • step 4: Draw the circuit • step 5: Check for DRC and ERC errors. • step 6: Save and minimize • step 7: Open T-spice. • Step 8: File->New • Step 9: Write the t-spice code and run the code, observe the waveform • step 10:stop
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram and Layout diagram  
8	Observation Table, Look-up Table, Output	

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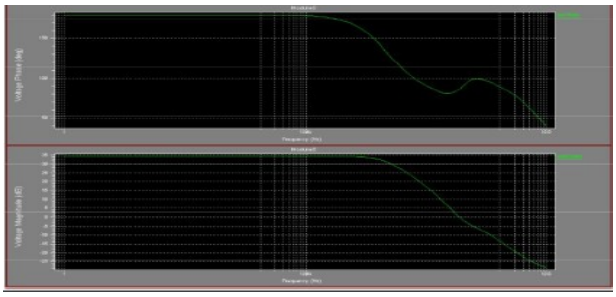
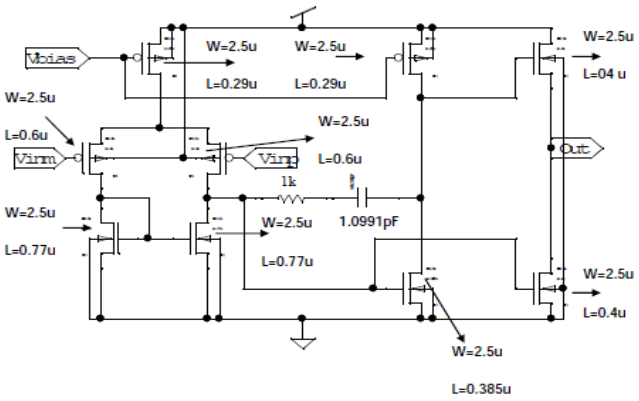
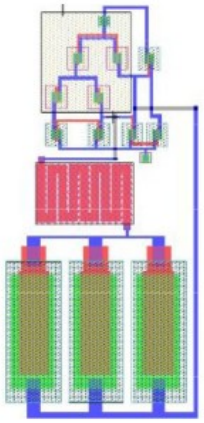
9	Sample Calculations	
10	Graphs, Outputs	
11	Results & Analysis	• The schematic and layout for the Single stage differential amplifier is successfully verified and tested.
12	Application Areas	• FET, Oscilloscopes, Electronic voltmeters, operational aplifiers
13	Remarks	
14	Faculty Signature with Date	

Experiment 15 :Comon Source Differential amplifier

-	**Experiment No.:**	15	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Common source differential amplifier						
2	Course Outcomes	Design common source differential amplifier schematic , Layout and verify LVS.						
3	Aim	Design an Common Source Differential amplifier with given specification, complete design flow mentioned below. a. Draw the schematic and verify the following. i)DC Analysis. ii)AC Analysis. b) Draw the Layout and verify the DRC, ERC						
4	Material / Equipment Required	Lab Manual						
5	Theory, Formula, Principle, Concept	Basic structure of CMOS circuits to design the given circuit						
6	Procedure, Program, Activity, Algorithm, Pseudo	• step 1: start • step 2: Double click on S-edit • step 3: File->New						

	Code	• step 4: Draw the circuit • step 5: Check for DRC and ERC errors. • step 6: Save and minimize • step 7: Open T-spice. • Step 8: File->New • Step 9: Write the t-spice code and run the code, observe the waveform • step 10:stop
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram and Layout diagram  
8	Observation Table, Look-up Table, Output	
9	Sample	

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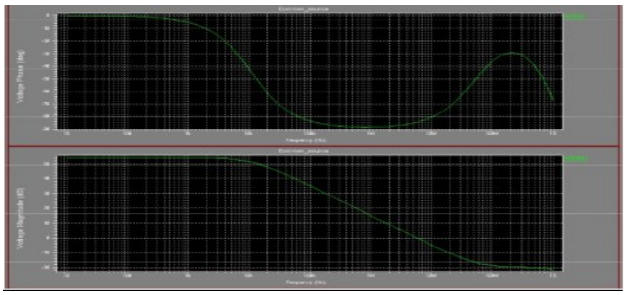
	Calculations	
10	Graphs, Outputs	
11	Results & Analysis	• The schematic and layout for the common source differential amplifier is successfully verified and tested.
12	Application Areas	• FET, Oscilloscopes, Electronic voltmeters, operational aplifiers
13	Remarks	
14	Faculty Signature with Date	

Experiment 16 :Comon Drain Differential amplifier

-	**Experiment No.:**	16	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Common drain differential amplifier						
2	Course Outcomes	Design common drain differential amplifier schematic , Layout and verify LVS.						
3	Aim	Design an Common Drain Differential amplifier with given specification, complete design flow mentioned below. a. Draw the schematic and verify the following. i)DC Analysis. ii)AC Analysis. b) Draw the Layout and verify the DRC, ERC						
4	Material / Equipment Required	Lab Manual						
5	Theory, Formula, Principle, Concept	Basic structure of CMOS circuits to design the given circuit						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• step 1: start • step 2: Double click on S-edit • step 3: File->New • step 4: Draw the circuit						

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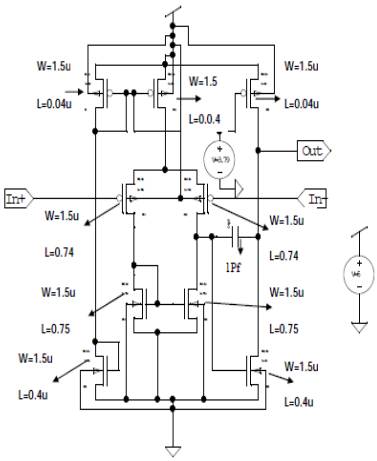
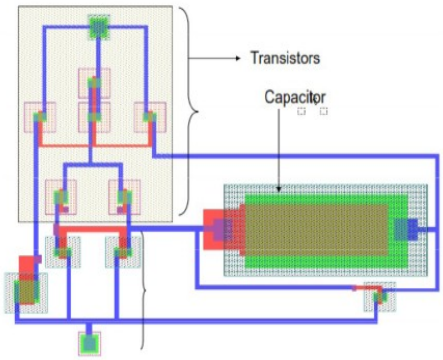
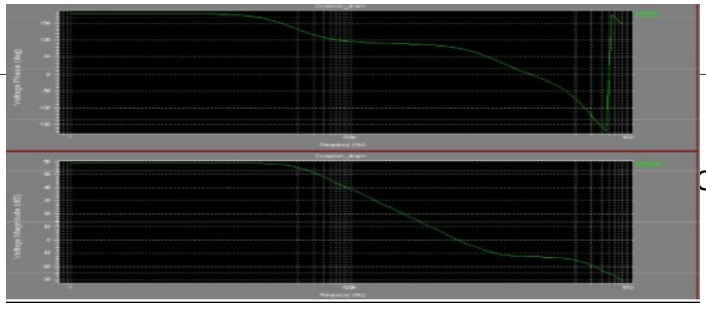
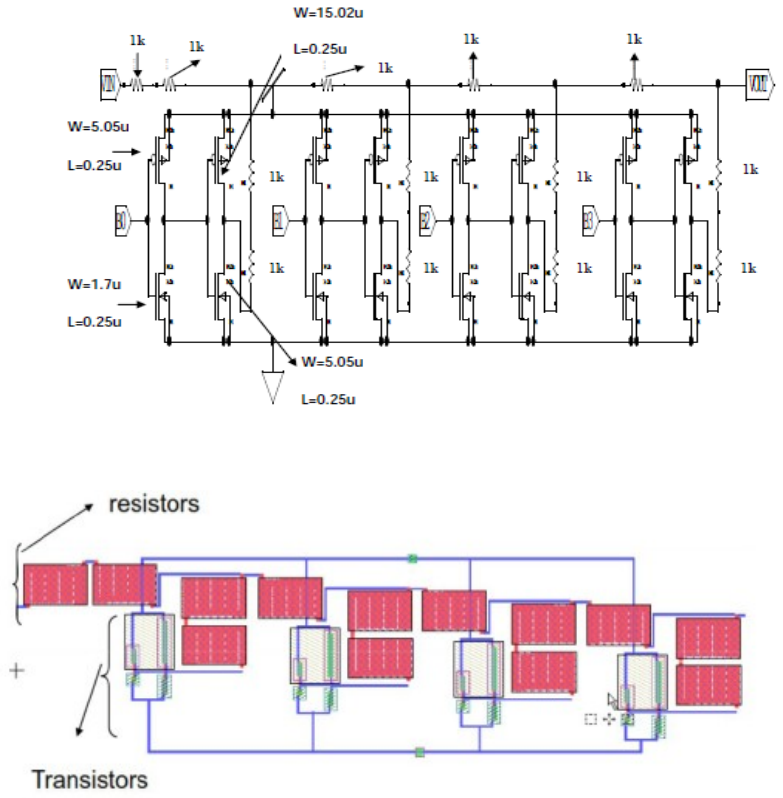
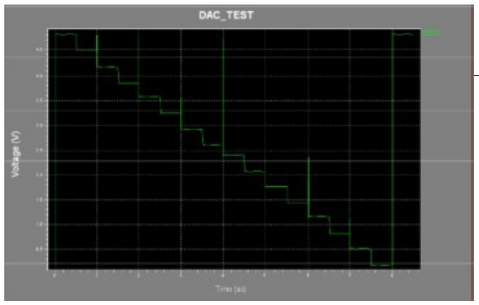
		• step 5: Check for DRC and ERC errors. • step 6: Save and minimize • step 7: Open T-spice. • Step 8: File->New • Step 9: Write the t-spice code and run the code, observe the waveform • step 10:stop
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram and Layout diagram  
8	Observation Table, Look-up Table, Output	
9	Sample Calculations	
10	Graphs, Outputs	

11	Results & Analysis	• The schematic and layout for the common drain differential amplifier is successfully verified and tested.
12	Application Areas	• FET, Oscilloscopes, Electronic voltmeters, operational aplifiers
13	Remarks	
14	Faculty Signature with Date	

Experiment 17 :R-2R DAC

-	**Experiment No.:**	17	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	R-2R DAC						
2	Course Outcomes	Design R-2R DAC schematic , Layout and verify LVS.						
3	Aim	Design an R-2R DAC with given specification, complete design flow mentioned below. a. Draw the schematic and verify the following. i)DC Analysis. ii)AC Analysis. b) Draw the Layout and verify the DRC, ERC						
4	Material / Equipment Required	Lab Manual						
5	Theory, Formula, Principle, Concept	Basic structure of CMOS circuits to design the given circuit						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• step 1: start • step 2: Double click on S-edit • step 3: File->New • step 4: Draw the circuit • step 5: Check for DRC and ERC errors. • step 6: Save and minimize • step 7: Open T-spice. • Step 8: File->New						

		• Step 9: Write the t-spice code and run the code, observe the waveform • step 10:stop
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Circuit Diagram and Layout diagram 
8	Observation Table, Look-up Table, Output	
9	Sample Calculations	
10	Graphs, Outputs	
11	Results & Analysis	• The schematic and layout for the R-2R DAC is successfully verified

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		and tested.
12	Application Areas	• Motor control, digital potentiometers, Software Radio, Data distribution system
13	Remarks	
14	Faculty Signature with Date	